

# DQDN15 AMD QUEEN M12

## Muxless /UMA Schematics Document

### AMD LIANO APU FS1

### AMD GPU Seymour XT

### FCH HUDSON M3

### PCB 10246-1

[www.aitech1.ru](http://www.aitech1.ru)

2011-05-28

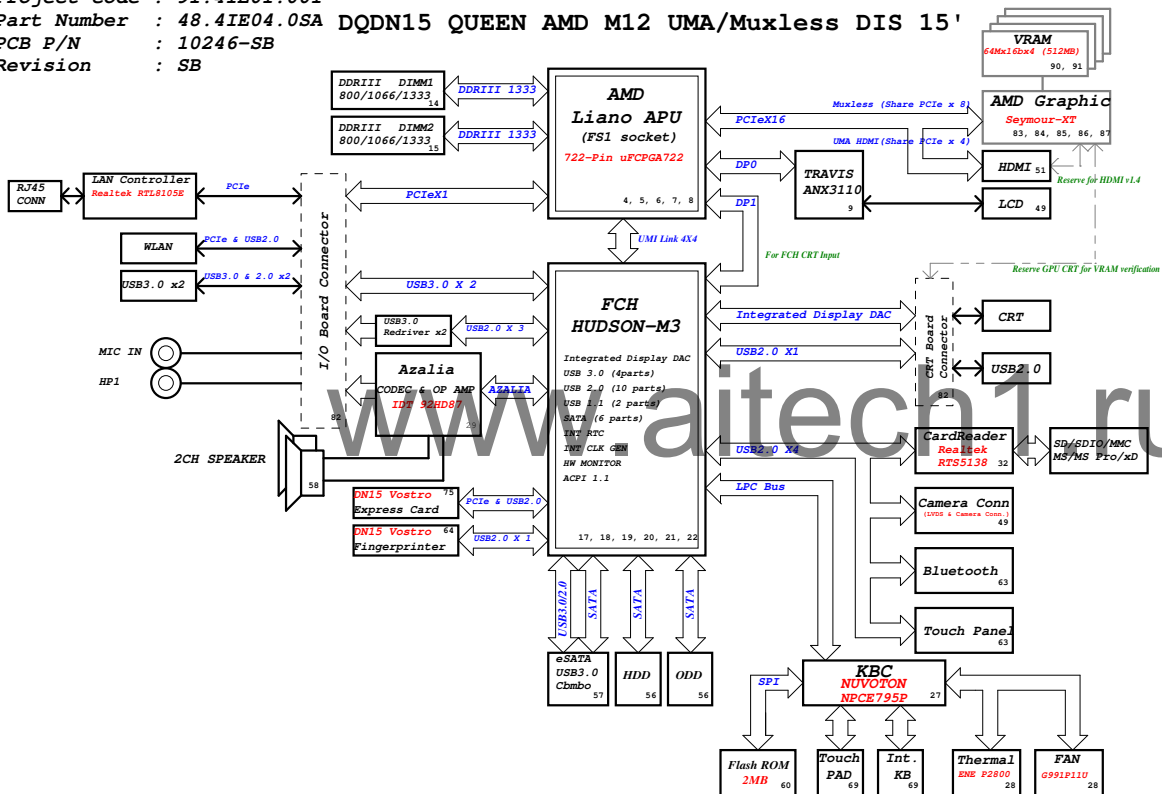
REV : A00

*DY :None Installed*  
*UMA\_PX:UMA and Muxless platform installed*  
*DIS\_PX:DIS and Muxless platform installed*  
*PX:Muxless platform installed*  
*FCH\_UMA\_PX:UMA\_PX CRT FCH output*  
*Whistler: For 8 X Vram*  
*DN15: For DN15*

DQ15 AMD DIS SAMSUNG T1

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		<b>Cover Page</b>	
Size Custom	Document Number <b>DQDN15 AMD QUEEN M12</b>	Rev <b>X00</b>	
Date: Friday, May 27, 2011		Sheet 1	of 104

Project code : 91.4IE01.001  
Part Number : 48.4IE04.0SA DQDN15 QUEEN AMD M12 UMA/Muxless DIS 15'  
PCB P/N : 10246-SB  
Revision : SB



<b>CHARGER</b> <b>BQ24745</b>		<b>40</b>
<b>INPUTS</b>	<b>OUTPUTS</b>	
<b>AD+</b> <b>BT+</b>	<b>DCBATOUT</b>	
<b>SYSTEM DC/DC</b> <b>TP551123</b>		<b>41</b>
<b>INPUTS</b>	<b>OUTPUTS</b>	
<b>DCBATOUT</b>	<b>3D3V AUX S5</b> <b>5V AUX S5</b> <b>5V S5</b> <b>3D3V S5</b>	
<b>APU Core/NB Power</b> <b>ISL6267BRTZ-T</b>		<b>42, 43</b>
<b>INPUTS</b>	<b>OUTPUTS</b>	
<b>DCBATOUT</b>	<b>APU VDD</b> <b>APU VDDNB</b>	
<b>DDRIII SUS</b> <b>TP55116RGER</b>		<b>44</b>
<b>INPUTS</b>	<b>OUTPUTS</b>	
<b>DCBATOUT</b>	<b>1D5V S3</b>	
<b>DDRIII VTT</b> <b>TP55116RGER</b>		<b>44</b>
<b>INPUTS</b>	<b>OUTPUTS</b>	
<b>DCBATOUT</b>	<b>0D75V S0</b>	
<b>APU VDDR/VDDEP</b> <b>R78209</b>		<b>46</b>
<b>INPUTS</b>	<b>OUTPUTS</b>	
<b>DCBATOUT</b>	<b>1D2V S0</b>	
<b>AMD FCH CORE Power</b> <b>R78209</b>		<b>46</b>
<b>INPUTS</b>	<b>OUTPUTS</b>	
<b>DCBATOUT</b>	<b>1D1V S5</b>	
<b>AMD GPU CORE</b> <b>R78208B</b>		<b>92</b>
<b>INPUTS</b>	<b>OUTPUTS</b>	
<b>DCBATOUT</b>	<b>VGA CORE PWR</b>	
<b>PCB LAYER</b>		
<b>L1: Top</b>		
<b>L2: VCC</b>		
<b>L3: Signal</b>		
<b>L4: Signal</b>		
<b>L5: GND</b>		
<b>L6: Bottom</b>		

## Strapping

No Fusion Config, Strap Not needed, but reserve

### REQUIRED SYSTEM STRAPS

	EC_PWM2 PCH GP0199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM DEFAULT	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

## USB Table

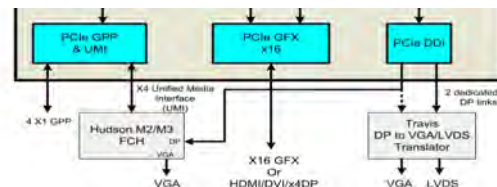
Pair	Device
0	USB Debug Port / CRT USB 2.0
1	Mini Card (WLAN)
2	Fingerprint
3	WWAN
4	Bluetooth
5	Touch Panel
6	eSATA/USB-Charger
7	CCD Camera
8	New Card
9	CardReader
10	USB 3.0 port 1
11	USB 3.0 port 2
12	USB 3.0 port 3
13	USB 3.0 port 4

## PCIe Routing

	APU
LANE0	LAN
LANE1	—WWAN—
LANE2	WLAN
LANE3	—CardReader—

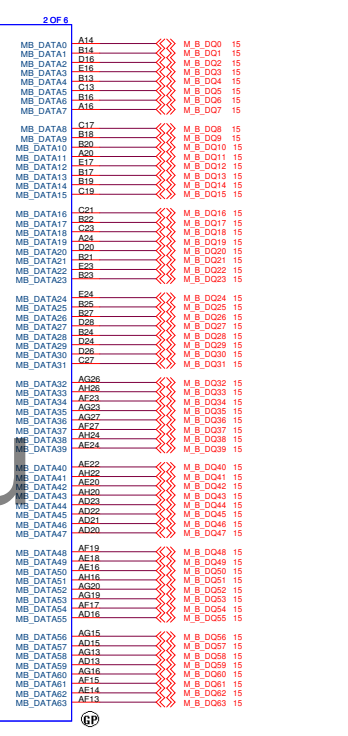
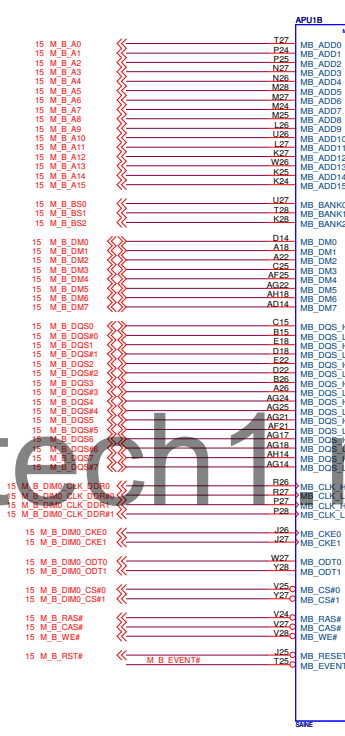
	FCH
LANE0	
LANE1	—Express Card—
LANE2	
LANE3	

DQ15 AMD D15 SAMSUNG TI



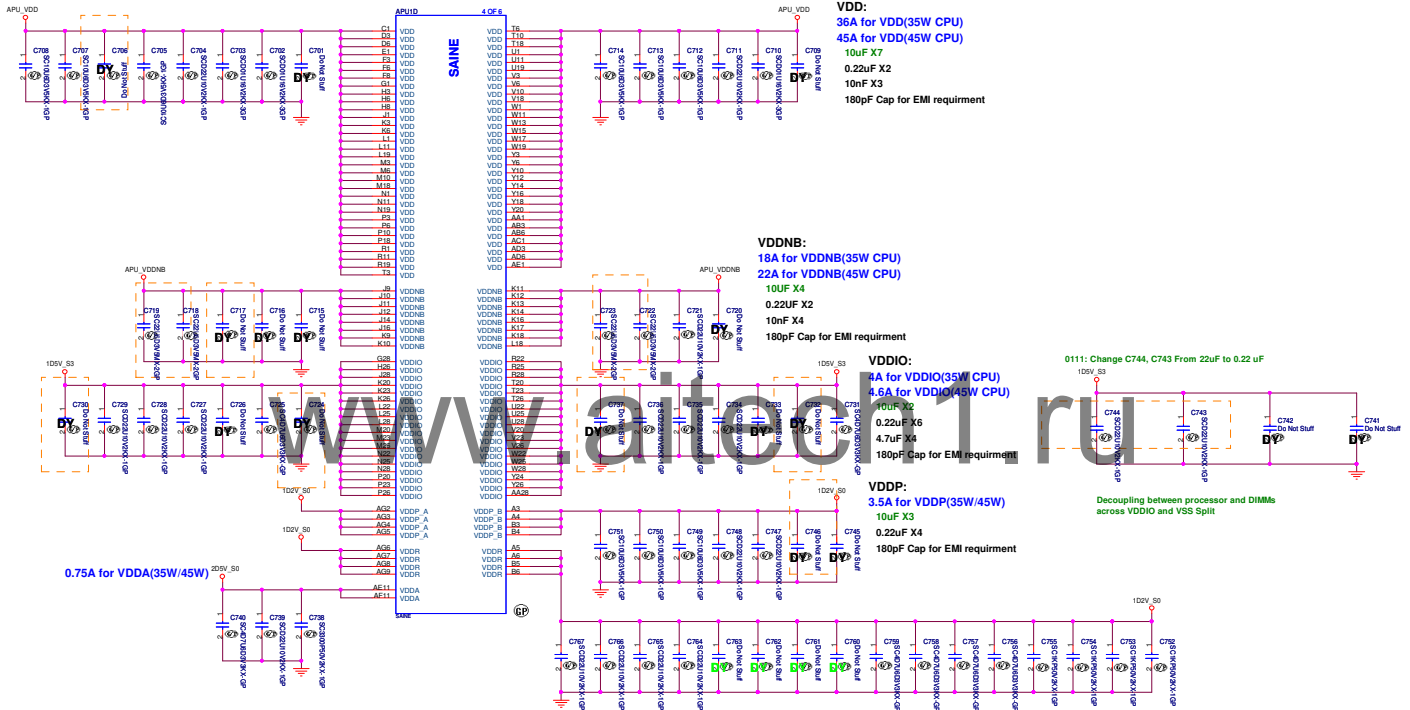
Title		<b>APU PCIE(1/5)</b>		Rev
Size A3	Document Number	<b>QUEEN AMD Muxless/UMA</b>		100
Date	Thursday May 26 2011	Sheet	4	of 104





Title				<b>APU_DDR(2/5)</b>				Rev	
Size		Document Number					X		
A3		<b>QUEEN AMD Muxless/UMA</b>							
Date: Thursday, May 26, 2011				Sheet 5		of		104	





**VDD:**  
36A for VDD(35W CPU)  
45A for VDD(45W CPU)  
10uF X7  
0.22uF X2  
10nF X3  
180pF Cap for EMI requirement

**VDDNB:**  
18A for VDDNB(35W CPU)  
22A for VDDNB(45W CPU)  
10uF X4  
0.22uF X2  
10nF X4  
180pF Cap for EMI requirement

**VDDIO:**  
4A for VDDIO(35W CPU)  
4.6A for VDDIO(45W CPU)  
10uF X2  
0.22uF X6  
4.7uF X4  
180pF Cap for EMI requirement

0111: Change C744, C743 From 22uF to 0.22 uF

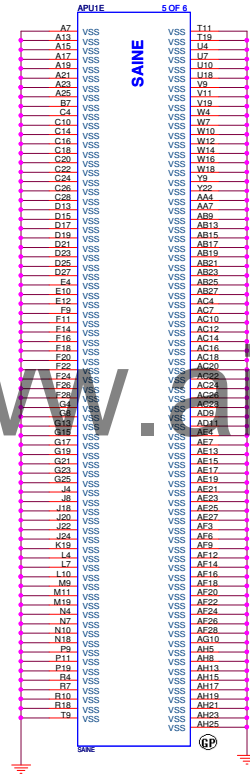
**VDDP:**  
3.5A for VDDP(35W/45W)  
10uF X3  
0.22uF X4  
180pF Cap for EMI requirement

Decoupling between processor and DIMMs  
across VDDIO and VSS Split

**VDDR:**  
3A for VDDR(35W)  
3.5A for VDDR(45W)  
4.7uF X4  
0.22uF X4  
1nF X4  
180pF Cap for EMI requirement

DQ15 AMD DIS SAMSUNG TI

<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 8F, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taiwan 301, Taiwan, R.O.C.			
File: <b>APU Power(4/5)</b>			
Rev	Document Number	Rev	
Customer	<b>QUEEN AND Muxess/UMA</b>	Rev	<b>X00</b>
Date: Thursday, May 28, 2015		Sheet	7 of 104



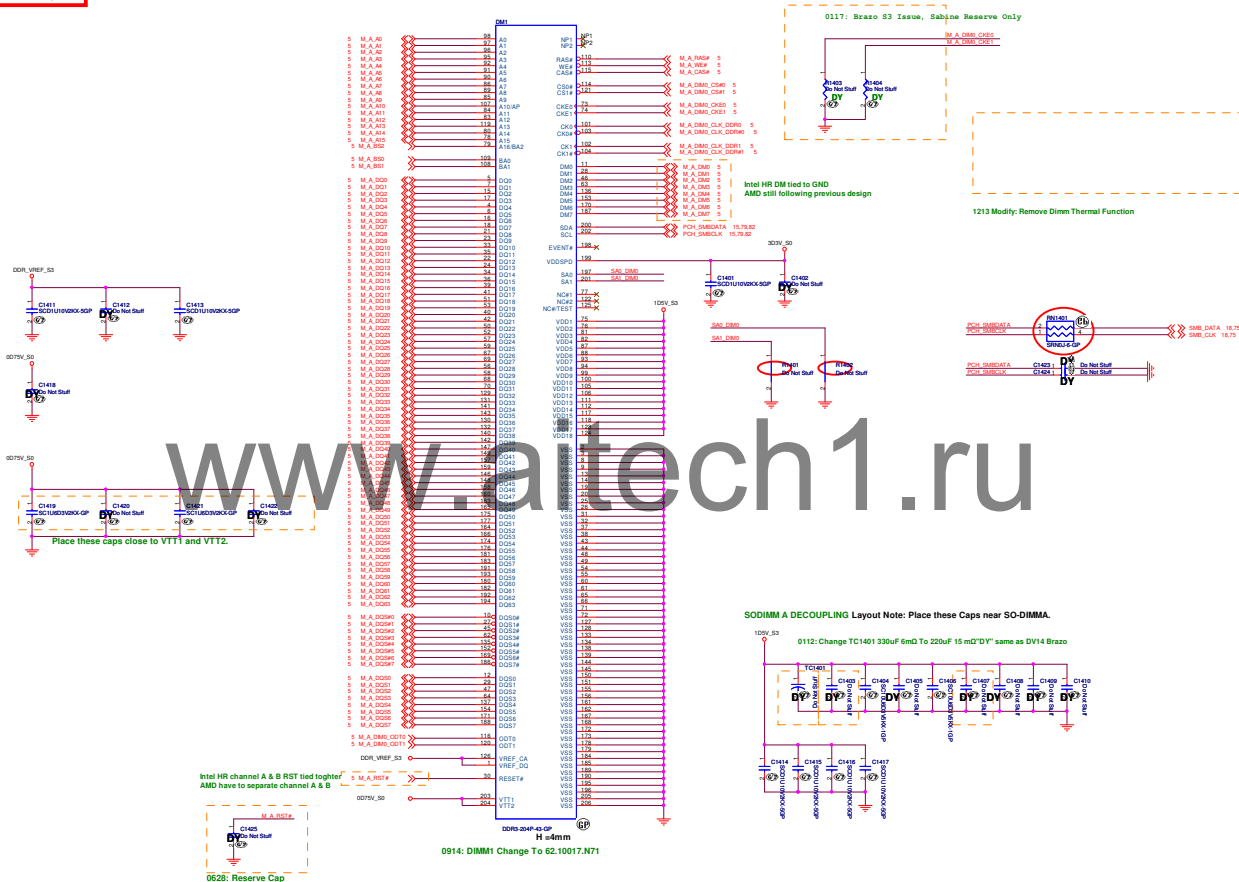
www.nitech1.ru

DQ15 AMD DIS SAMSUNG T1

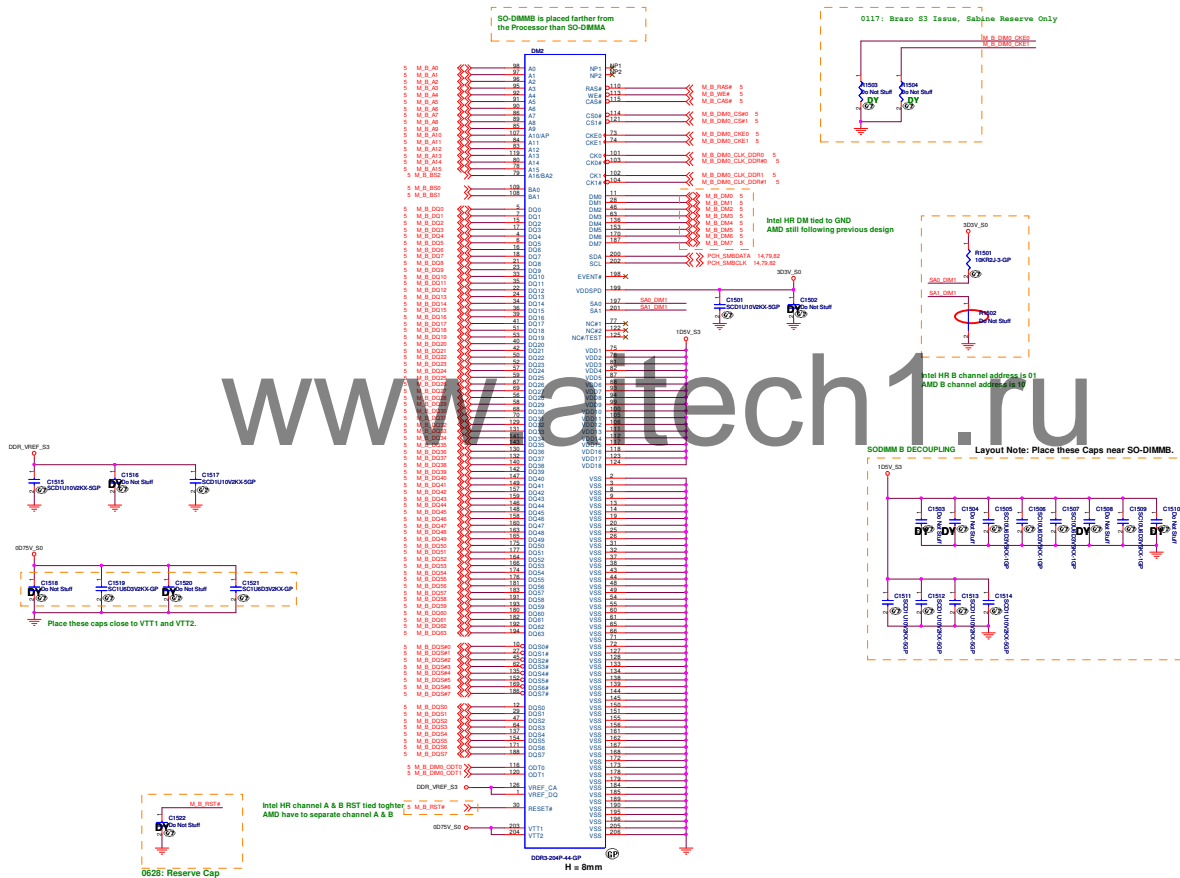
<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>APU VSS(5/5)</b>			
Size	Document Number	Rev	
A5			
<b>QUEEN AMD Muxless/UMA00</b>			
Date:	Thursday, May 26, 2011	Sheet	6 of 104

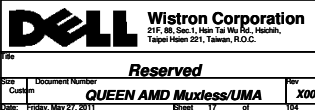


SSID = MEMORY



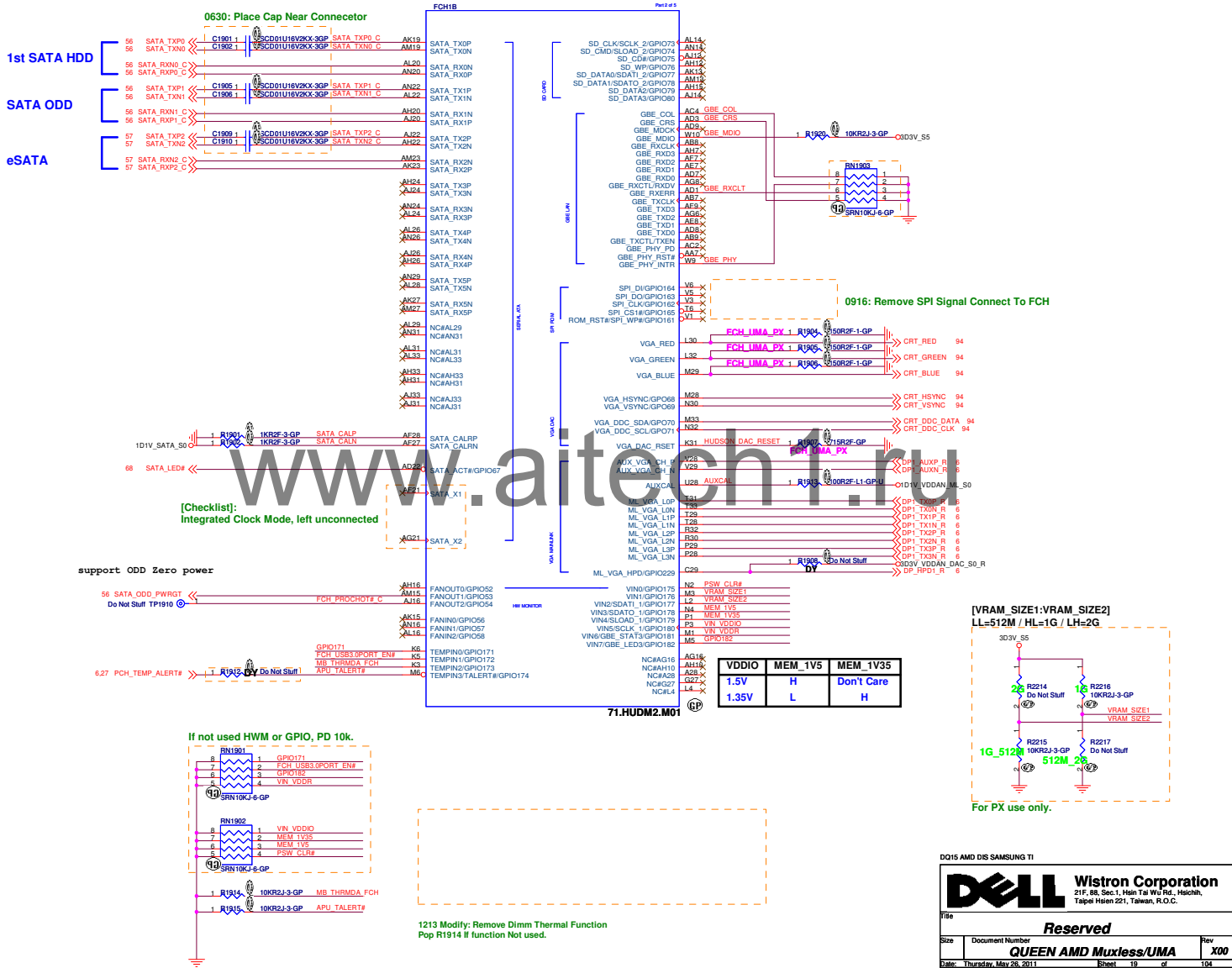
SSID = MEMORY









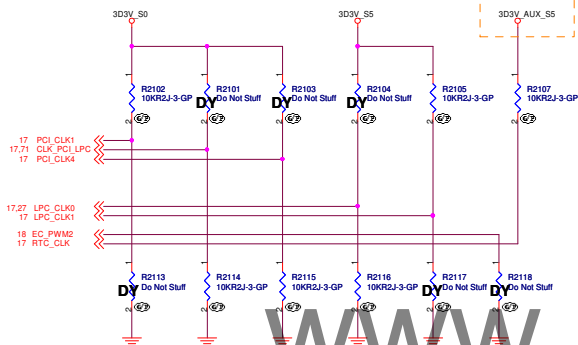




SSID = S.B

## REQUIRED STRAPS

CRB: PU to 3.3V\_AUX\_S5  
Checklist: PU to 3.3V\_S5  
Confirm with AMD, follow CRB suggestion



## REQUIRED SYSTEM STRAPS

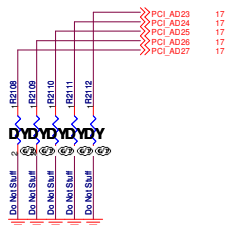
Use this pin to determine INT/EXT CLK

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCH_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal)
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

No Fusion Config, Strap Not needed, but reserve

Ball Name	Strap Function	Description
EC_PWM2	ROM Type	SPI ROM: 2.2-KΩ 5% pull-down LPC ROM: Pull-up to 3.3V <sub>S5</sub> . External pull-up resistor is not required as FCH has integrated 10-KΩ pull-up to 3.3V <sub>S5</sub> .

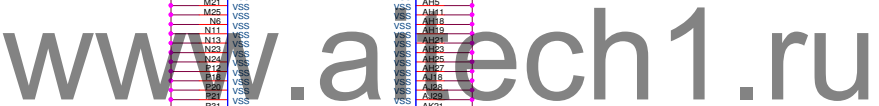
## DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI\_AD[27:23]

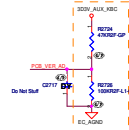
DQ15 AMD DIS SAMSUNG T1



Title			
<b>Reserved</b>			
Size A3	Document Number		Rev
<b>QUEEN AMD Muxless/UMA</b>			
Date: Thursday, May 26, 2011	Sheet	22	of 104

SSID = KBC

0107: Change R2724 & R2726 from 5% to 1% Resistor tolerance.

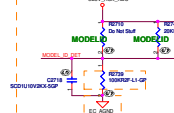


PCB VERSION A (UPP000)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100kΩ	10kΩ	3.0V
SB	100kΩ	20kΩ	2.75V
SC	100kΩ	250kΩ	2.60V
SD	100kΩ	47kΩ	2.25V
SE	100kΩ	64.9kΩ	2.0V
SE	100kΩ	76.8kΩ	1.8V
SE	100kΩ	100kΩ	1.65V

0107: POP C2718, R2728, Change To Voltage Divider

+ BCM Control For R2710 Value

Default R2710 10k ±D01P LMA



0702 Modify:

Default on-stuff R2728 (Internal PL in KBC)

0107: Update Model, ID, DET

D01P, AND, UMA

D01P, AND, D01P (FX)

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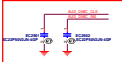
D01P, AND, D01P (FX)

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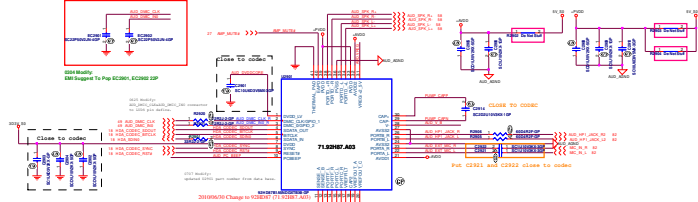


0413 R01 Modify:  
Add R2020, P2020 and reserved EC2001, EC2002 on  
AUD\_SMMC, CLK, BAUD\_SMMC, RD for EMC suggestion.  
0165 Modify:  
EMM Reserve R2020, R2021 Place Near L.C.D1 Connector.  
Move EC2001 + EC2002 to P-40 and place after R2020, R2021  
0165 Modify:  
Vendor Suggest To Change R2020 To 33 Ohm

## For EMI



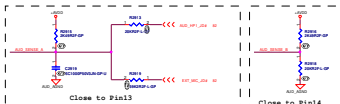
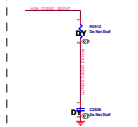
0164 Modify:  
EMM Suggest To Pop EC2001, EC2002 20P



AUD\_PC\_BEEP  
Trace width > 15 mils

AUD\_PC\_BEEP  
Trace width > 15 mils

## Azalia I/F EMI



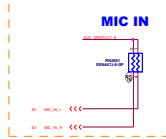
Close to Pin13

Close to Pin14

0165 EMM Reserve, Place Near R2018



0115: Move To M8



ANNIE Audio solution

www.aitech1.ru

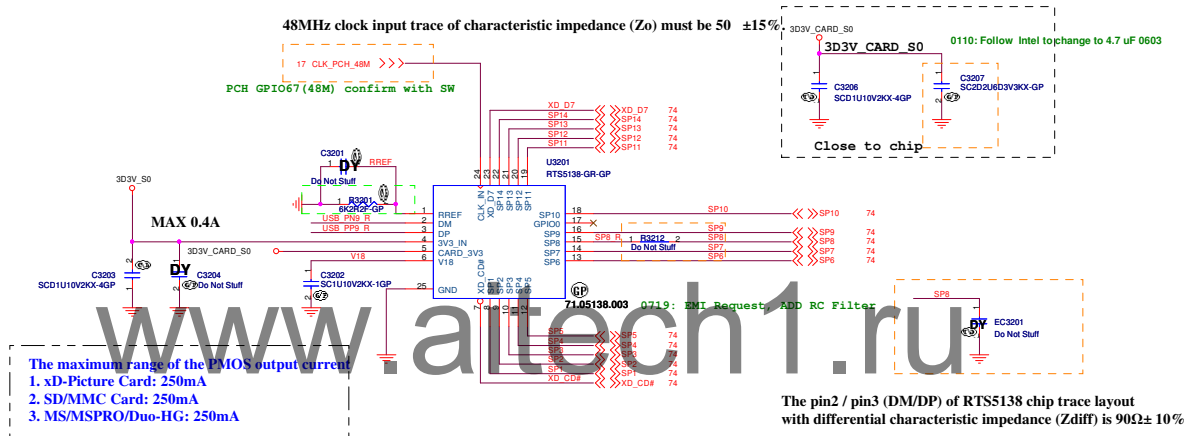
Remove Annie Audio

0016 AND 0016 EMI/EMC



**SSID = SDIO**

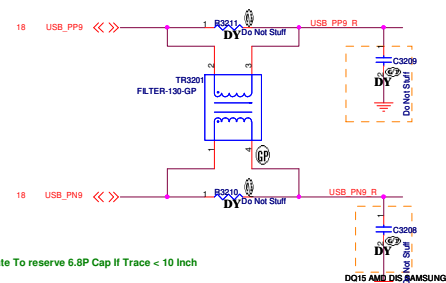
48MHz clock input trace of characteristic impedance ( $Z_0$ ) must be  $50 \pm 15\%$



**The pin2 / pin3 (DM/DP) of RTS5138 chip trace layout with differential characteristic impedance ( $Z_{diff}$ ) is  $90\Omega \pm 10\%$**

## POWER TRACE

- 1.RT5138: pin 4 (3V3\_IN) trace fixed width is 30 mils (minimum).
  - 2.RT5138: pin 5 (CARD\_3V3) trace fixed width is 30 mils (minimum).
  - 3.RT5138: pin 6 (V18) trace fixed width is 12 mils (minimum).
- Keep the trace routing lengths as short as possible.
- 4.RT5138: pin 1 (RREF) trace fixed width is 12 mils (minimum).
  - 5.RT5138: pin 1 (RREF) trace must far away 48MHz clock trace.
- 6.De-coupling and Bulk capacitor should place near to RT5138 chip and Combo Socket.
- 7.It is recommended that use of ferrites bead on power trace.
- 8.Via size: Pad>=32 mils, Finished hole>=16 mils,



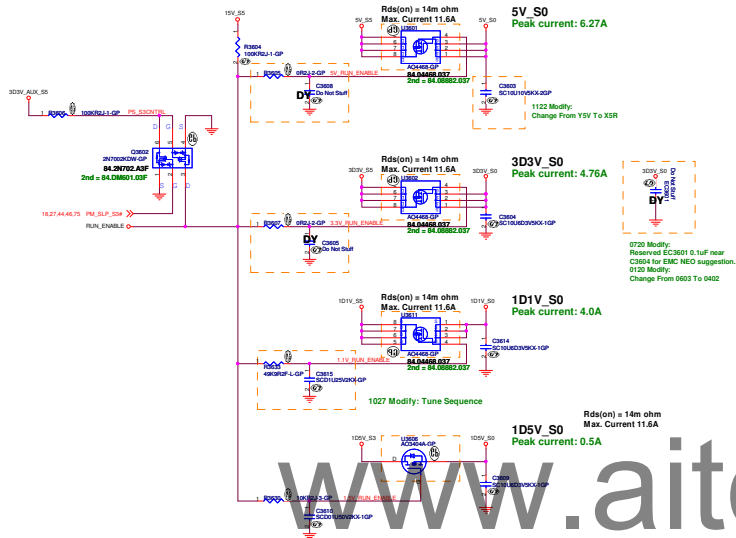
0103 Modify:  
AMD Spec Update To reserve 6.8P Cap If Trace < 10 Inch

0118 Modify:  
Change TR3201 To 69.10118.001 due to layout limitation

DQ15 AND DIS SAMSUNG T

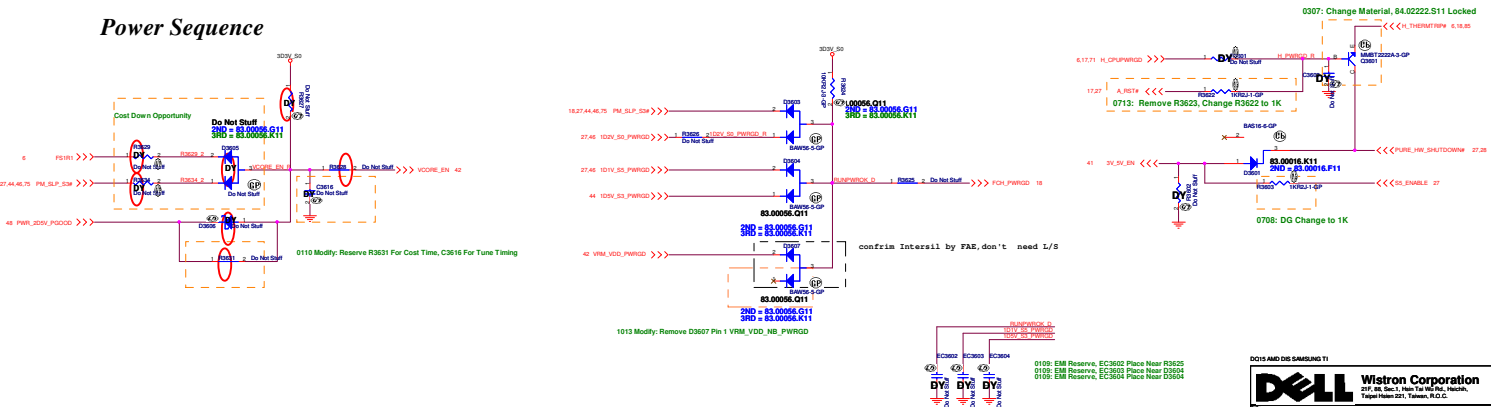


# ROSA Run Power



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## Power Sequence



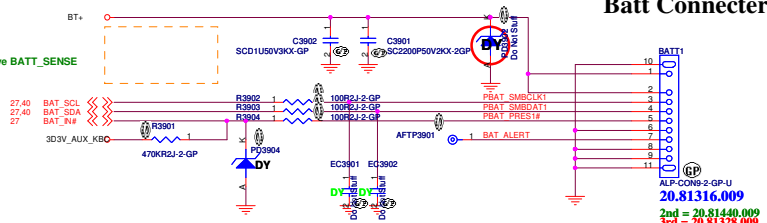
DDIS AND DIS SAMUNG 11

**DELL** Wistron Corporation  
2/F, 38, Sec. 1, Hsin-Tai Rd, N. T. Hsinchu, Taiwan, R.O.C.

Power On Logic  
QUEEN AMD Muxless/UMA  
X200

SSID = BATT CONN

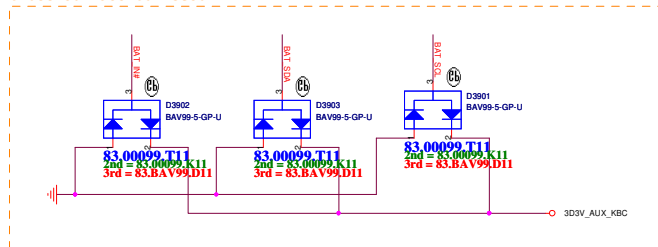
0916: Change Charger IC, Remove BATT\_SENSE



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For actual location, need to be swap all pin

Close to Batt Connector



DQ15 AMD DIS SAMSUNG TI

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File			
<b>BATT CONN</b>			
Size A3	Document Number		Rev X
<b>QUEEN AMD MUXLESS/UMA</b>			
Date: Thursday, May 26, 2011	Sheet 39 of 104		

SSID = Charger

EE need pull high and net name  
0802 Rename H\_PROCHOT#

6.27 H\_PROCHOT#

X00 0415

X00 0415

X00 0415

EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HWK2
65W	0	0
90W	1	0
130W	0	1

0120 Modify

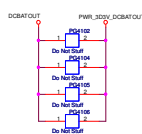
EE need check pull high

6222: Change PC4004, PC4024 From 6603 To 0402 0.1uF  
6106: Update PU4005 Symbol From Database.

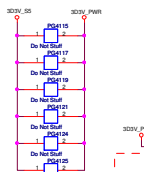
Charger Current=1.4~3.6A

DO15 AND DO2 SAMSUNG 11

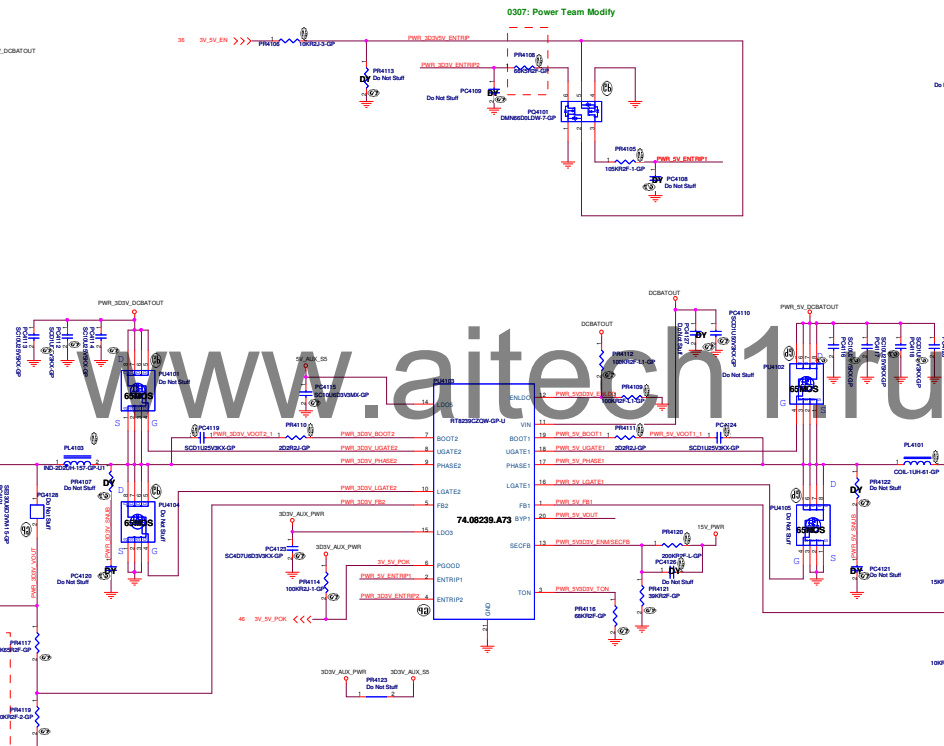
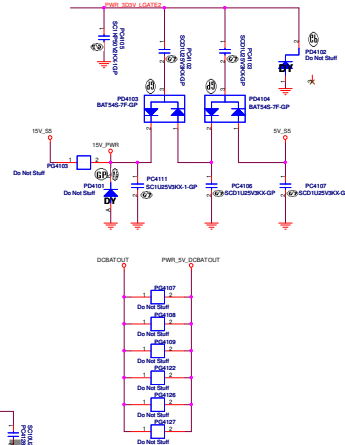
```
SSID = PWR.Plane.Regulator_3p3v5v
```



Design Current = 4.5A  
6.3A < OCP < 7.65A

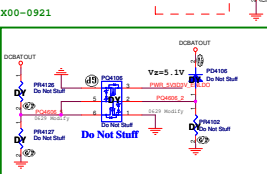


Design Current = 8.085A  
11.3A<OCP<13.7 A

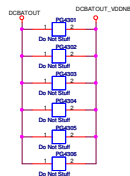


I/F cap: 10U 25V K05 X5R/ 78.10622.51L  
Inductor: 3.2U PCM063T-2R2Mh Cyntec 18mohm/20mohm Isat -14Rms 68.2R210.20Q  
O/F cap: 320U 6.3V MP6VU330CM5R7 15mOhm 3.16Rms Matsuki Polymer/77.53371.04L  
H/S: A04496 / 21mohm/26mOhm84.5Vg/s / 84.04496.037  
L/S: A04720L / 14mohm/ 17.5mOhm84.5Vg/s / 84.04720.037

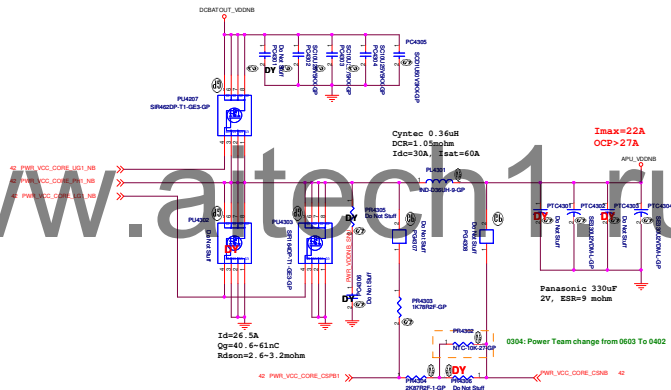
I/F cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: 2.2UPCMB104T-2R2MS Cyntec 6mohm/7mohm Isat -18Arms 6.2R210.20J  
O/P cap: 330U 6.3V MP6V3030M3C5R7 15mohm 3.16Arms Matsuki Polymer/77.53371.04L  
H/S: RKJ03B9DPA / 10.9mohm/15.1mohm/4.5Vsq/ 84.0003B9.B37  
L/S: RKJ03D4DPA / 4.6mohm/5.6mohm/4.5Vsq/ 84.00034.A37







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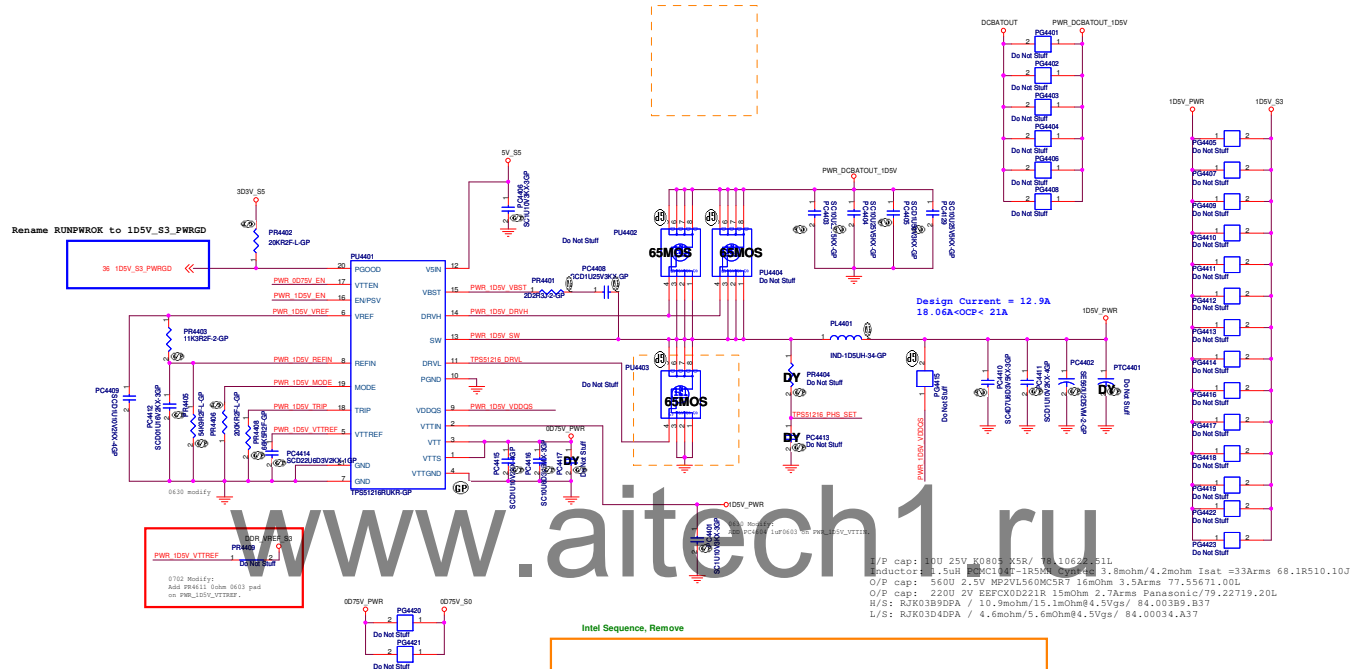


QD15 AMD DIS SAUSUNG TI



Document Number		Rev
QUEEN AMD Muxless/UMA		X00
Rev	1	1

SSID = PWR.Plane.Regulator\_1p5v0p75v

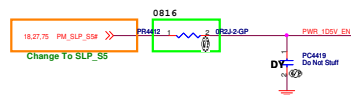
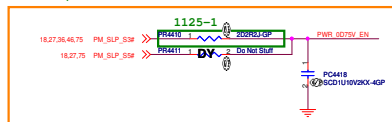


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE		
PR4406	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	



Add For Sequence

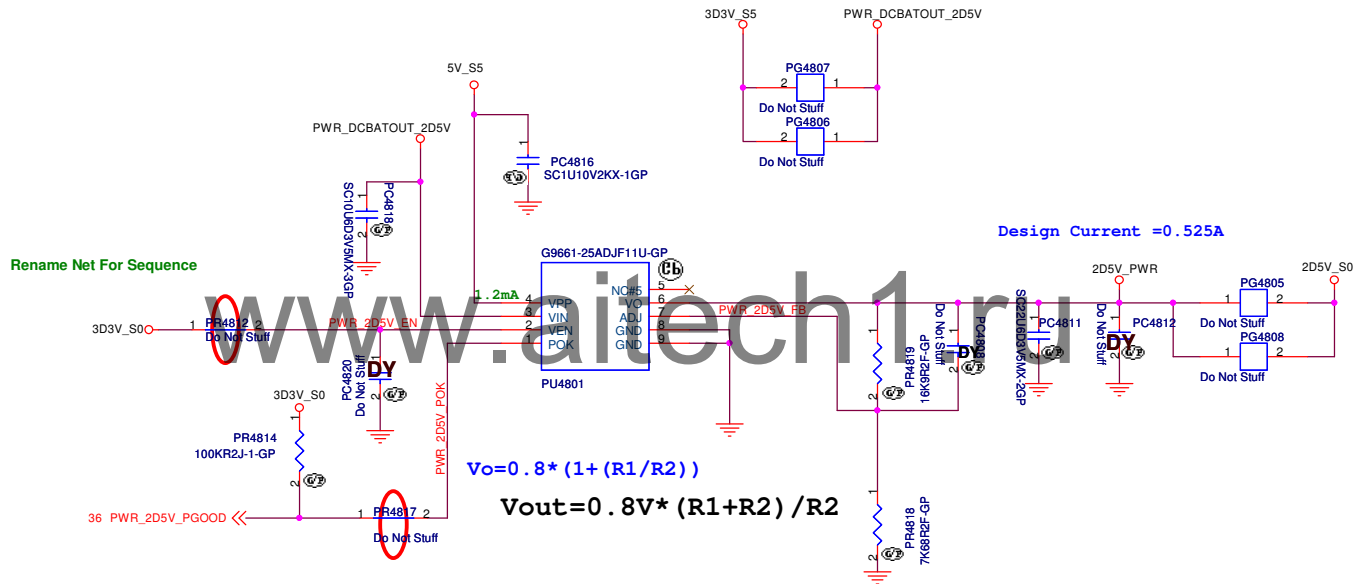






```
SSID = PWR.Plane.Regulator_2p5v VGA 1V
```

# G9661 for 2D5V\_S0



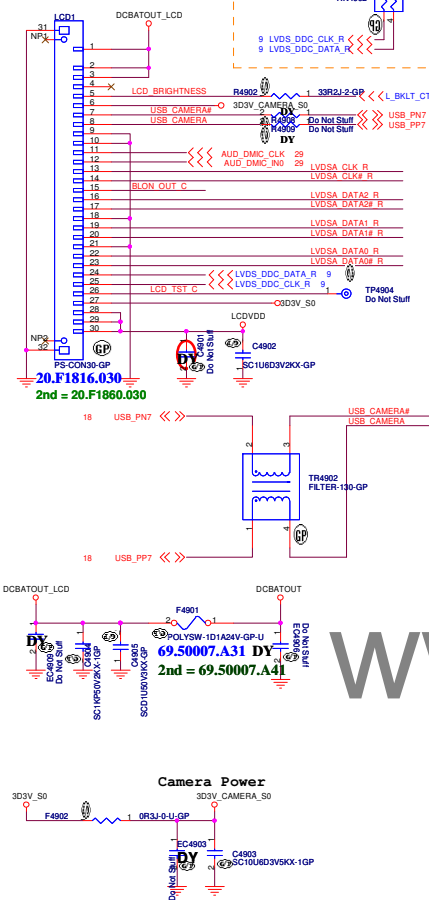
DQ15 AMD DIS SAMSUNG TI



0921Modify:  
Change BLON\_OUT\_C to pin 15 and pin 4  
to NC on LCD1.

0914 Modify:  
Change PU From Page 82 To Page 49

## LVDS CONNECTOR



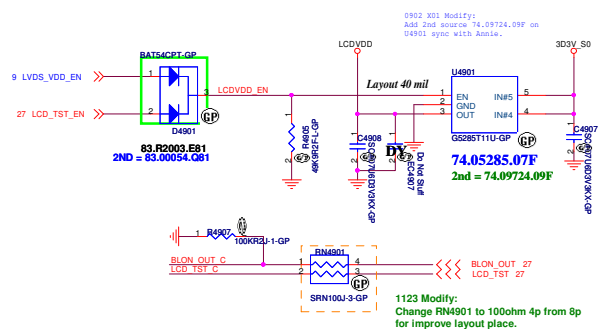
## (MB Pin Define)

MB CONN. (WIRE)	
Pin 1	DCBATOUT_LCD
Pin 2	DCBATOUT_LCD
Pin 3	DCBATOUT_LCD
Pin 4	BLON_OUT_C
Pin 5	LCD_BRIGHTNESS
Pin 6	3D3V_CAMERA_S0
Pin 7	USB_CAMERA#
Pin 8	USB_CAMERA
Pin 9	GND
Pin 10	GND
Pin 11	AUD_DMIC_CLK
Pin 12	AUD_DMIC_IN0
Pin 13	LVDSA_CLK
Pin 14	LVDSA_CLK#
Pin 15	LCD_DET_G
Pin 16	LVDSA_DATA2
Pin 17	LVDSA_DATA2#
Pin 18	GND
Pin 19	LVDSA_DATA1
Pin 20	LVDSA_DATA1#
Pin 21	GND
Pin 22	LVDSA_DATA0
Pin 23	LVDSA_DATA0#
Pin 24	LVDS_DDC_DATA_R
Pin 25	LVDS_DDC_CLK_R
Pin 26	LCD_TST_C
Pin 27	3D3V_S0
Pin 28	LCDVDD
Pin 29	LCDVDD
Pin 30	LCDVDD

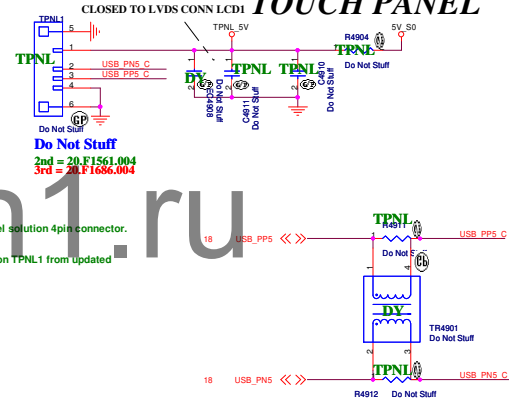
For EMI request  
Close to LVDS connector

SSID = VIDEO

LCD POWER for ROSA

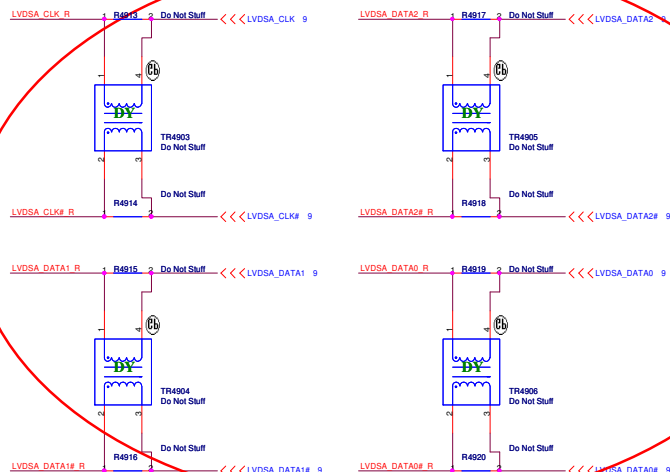


## TOUCH PANEL



0909 Modify:  
Add TPNL1 for touch panel solution 4pin connector

0928 Modify:  
Change To 20.F1621.004 on TPNL1 from updated  
connector list.



DQ15 AND DIS SAMSUNG T

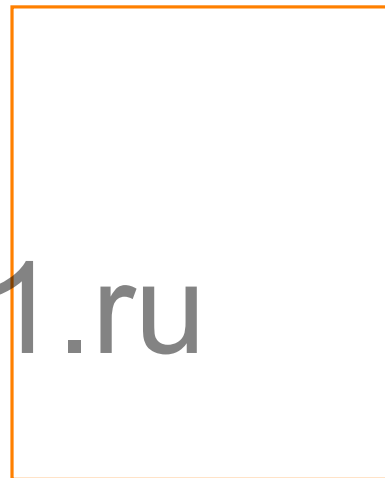
**DELL** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>LCD/Inverter Connector</b>			
Size	Document Number		Rev
Custom	<b>QUEEN AMD Muxless/UMA</b>		X
Date: Thursday, April 21, 2011	Sheet 49	of	104

Remove For M12 Spec & Put In Daughter BD



Remove For M12 Spec & Put In Daughter BD



Remove For M12 Spec & Put In Daughter BD



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DQ15 AMD DIS SAMSUNG TI



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**CRT Board Connector**

Size Document Number  
Custom

**QUEEN AMD Muxless/UMA**

Rev  
**X00**

Date: Thursday, May 26, 2011

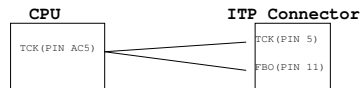
Sheet 50 of 104

Outputs are open drain and 5-V tolerant. External pull-up resistors to 5 V are required. These signals must be pulled high (to 3.3 V or 5 V) before VDDC is powered up.

SSID = User.Interface

### ITP Connector

H\_CPURESET use pull-up Resistor close  
ITP connector 500 mil (max ),  
others place near CPU side.

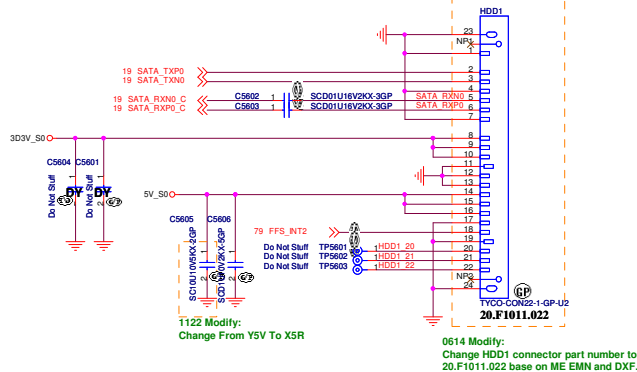


DQ15 AMD DS SAMSUNG TI

<b>DELL</b>			<b>Wistron Corporation</b> 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsuehshih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>ITP</b>					
Size A3	Document Number <b>QUEEN AMD Muxless/UMA</b>				Rev <b>X00</b>
Date: Thursday, May 28, 2011		Sheet 56 of 104			

SSID = SATA

## SATA HDD Connector

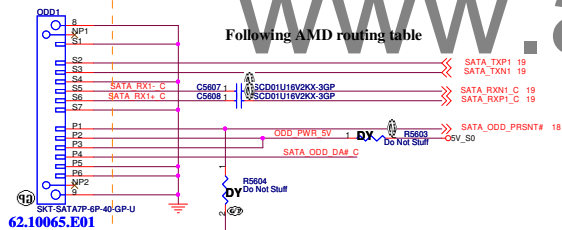


## ODD Connector

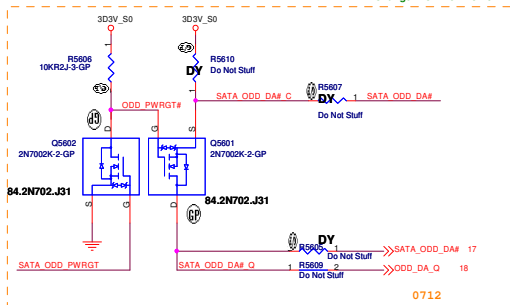
SATA\_RX- and SATA\_RX+ Trace  
Length match within 20 mil

When the drive is powered on, the FET to the MD/DA pin drive is OFF.  
When the drive is powered off, the FET to the MD/DA pin is ON

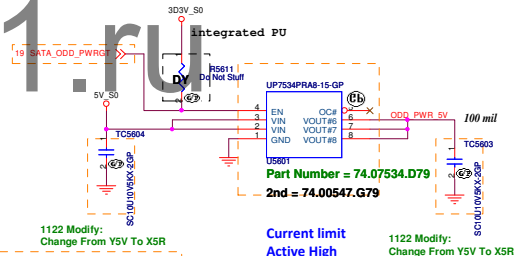
### SUPPORT ZERO SATA ODD



### 0719: Modify Zero ODD Circuit



### 1122 Modify: Change From Y5V To X5R

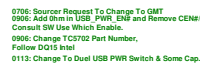


### 0109: EMI Request.



DQ15 AMD DES SAMSUNG TI

		<b>Wistron Corporation</b> 2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
		<b>HDD/ODD</b> <b>QUEEN AMD Muxless/UMA</b>	
File	Size	Document Number	Rev
	A3		X00
Date:	Thursday, May 28, 2011	Sheet	56 of 104



Switch Control Bit:  
CB=0 (AM):auto detection charger identification active  
CB=1 (PM):connect DP/DM to TDP/TDM.

0914: Remove Non Charger Co-lay Resistor.

30	31	
0	0	Auto
1	1	
2	2	
3	3	
4	4	De C. connessa a. V. L.



SSID = AUDIO

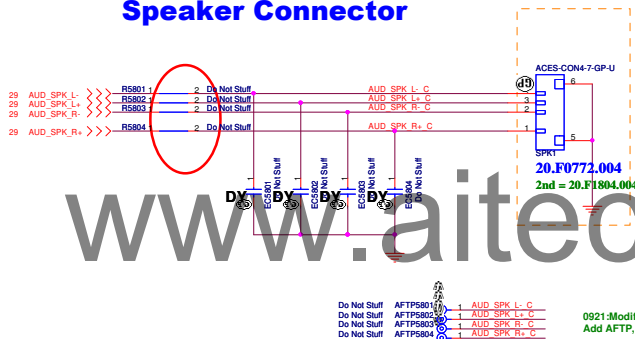
0715 Modify:  
Change ECS801-EC5804 to 100p 0402  
and default un-stuff.  
Add R5801-R5804 between SPK signal and connector  
for EMC NEO suggest.

0914 Modify:  
Change SPK1 to 20.F0772.004 from  
20.F1647.004 from Double updated.

0921 Modify:  
Modify Pin Define Base On DQ15 Intel

1110 X02 Modify:  
Add 2nd 20.F1804.004 on SPK1 from  
ME updated connector list.

## Speaker Connector



MB CONN. (WIRE)	
Pin 4	AUD_SPK_L-C
Pin 3	AUD_SPK_L+C
Pin 2	AUD_SPK_R-C
Pin 1	AUD_SPK_R+C

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0921 Modify  
Add AFTP, Follow DQ15 Intel

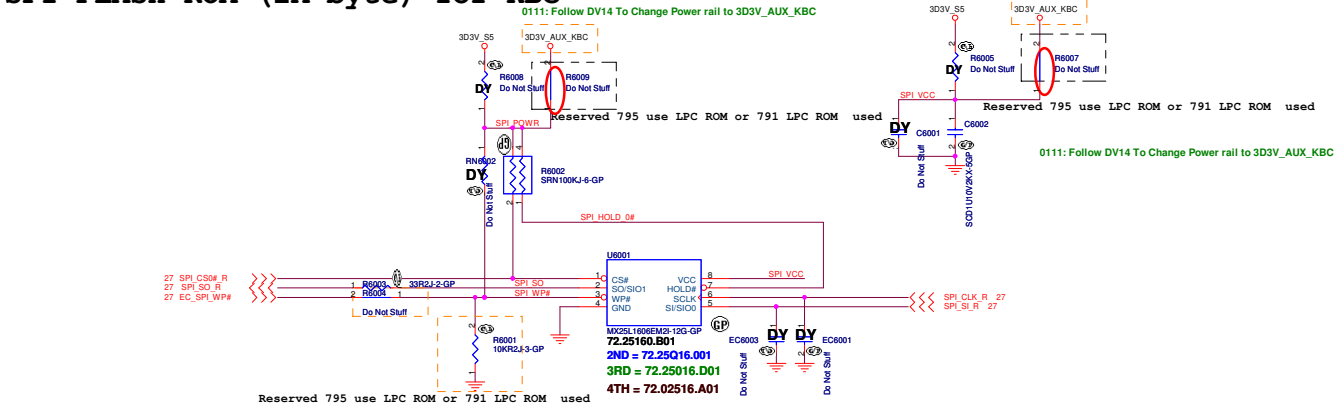
DQ15 AMD DIS SAMSUNG TI

**DELL** Wistron Corporation  
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File  
Size A3 Document Number  
Date: Thursday, May 26, 2011 Sheet 58 of 104  
Rev X00  
Audio Jack  
QUEEN AMD Muxless/UMA

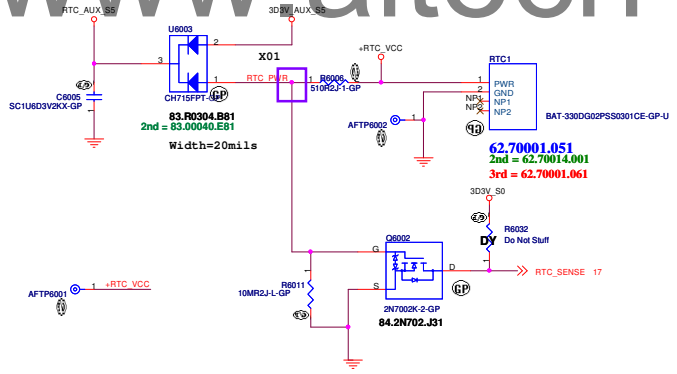
SSID = Flash.ROM

SPI FLASH ROM (2M byte) for KBC



SSID = RBATT

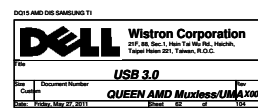
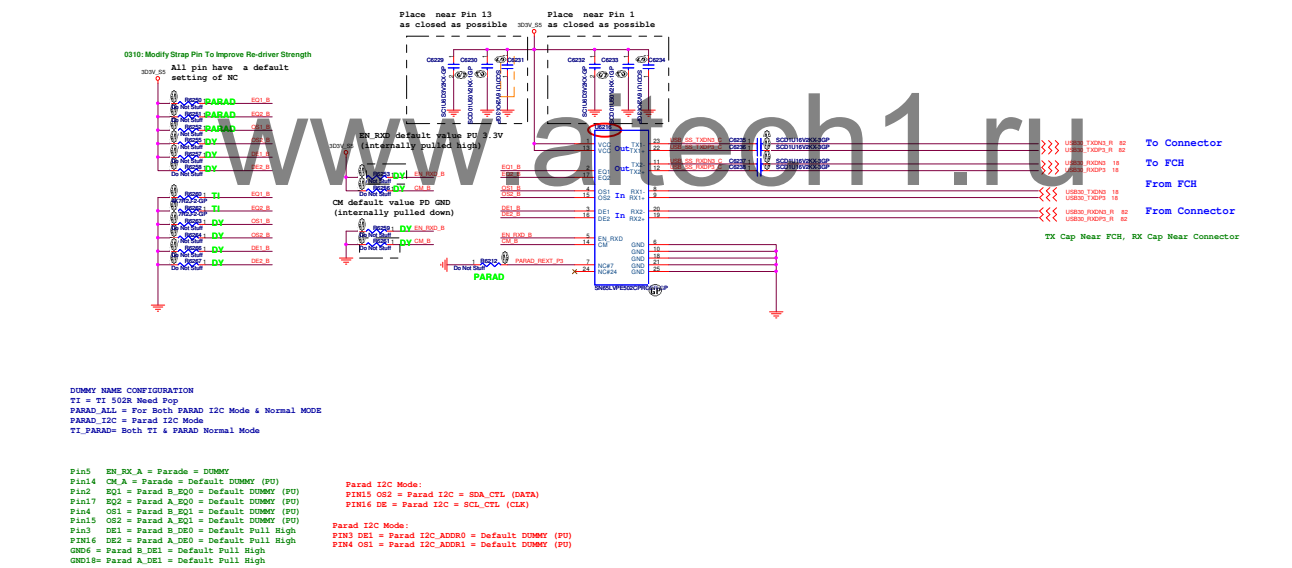
www.aitech1.ru



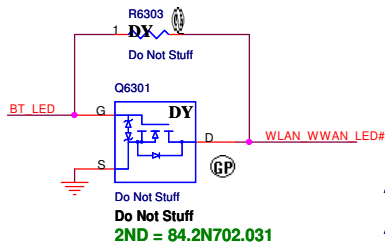
0105 Modify:  
updated RTC1 symbol and footprint from  
data base.  
1122 Modify:  
Add Q6002, R6010, R6011 for FACTORY RTC detect function.  
0111: Change RTC Schematic As DV14 Brazo, SW Suggest.

DQ15 AMD DES SAMSUNG TI

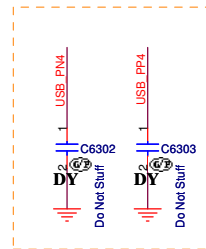
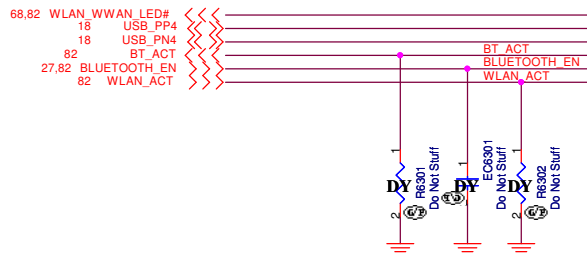
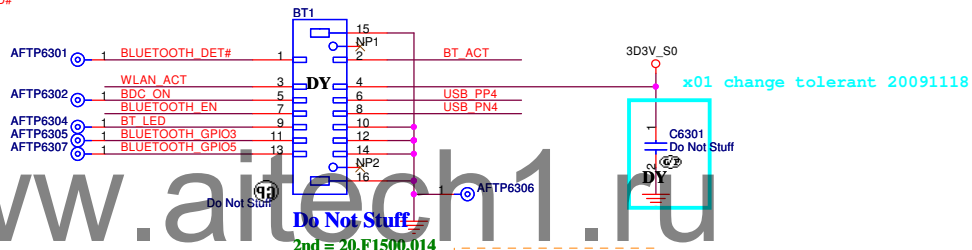
<b>DELL</b>		<b>Wistron Corporation</b> 2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipex Hsien 301, Taiwan, R.O.C.	
<b>Flash/RTC</b>			
File	Document Number	Rev	
A3	QUEEN AMD Muxless/UMA	X00	
Date:	Thursday, Mar 28, 2011	Sheet	60 of 104



# SSID = User.Interface



## Bluetooth Module conn.



AFTP6309	1	WLAN_ACT
AFTP6310	1	BLUETOOTH_EN
AFTP6308	1	BT_ACT
AFTP6311	1	3D3V_S0
AFTP6312	1	USB_PP4
AFTP6313	1	USB_PN4

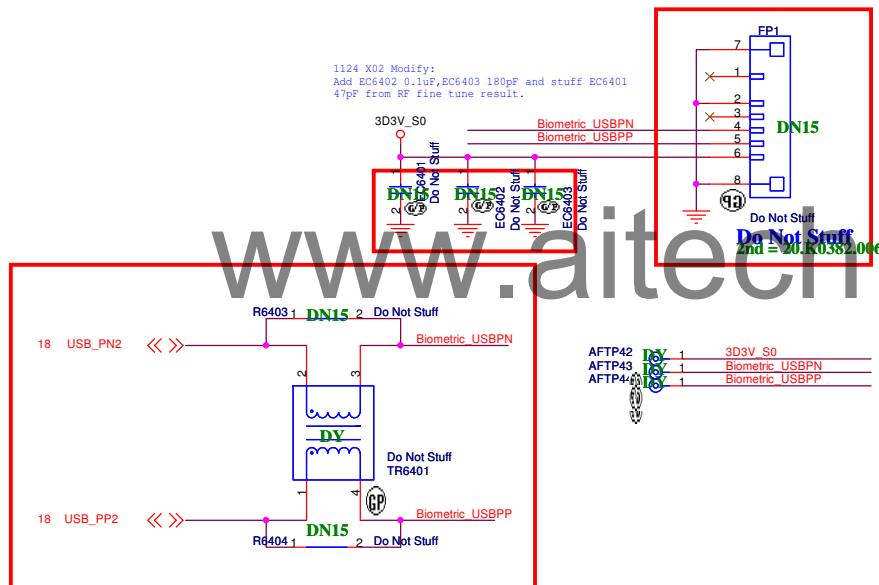
0906 Modify:  
 Dell Peter already confirmed DQ15 and DN15 will not support Bluetooth BT365, only support combo Wireless+BT. Please DUMMY Bluetooth connector(BT1) and stand off (HBT1) and related components.

0103 Modify:  
 AMD Spec Update To reserve 6.8P Cap If Trace < 10 Inch

DQ15 AMD DIS SAMSUNG TI

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Bluetooth</b>			
Size A4	Document Number <b>QUEEN AMD Muxless/UMA</b>		Rev <b>X00</b>
Date: Thursday, May 26, 2011	Sheet 63		of 104

## Finger Printer Connector



MB_CONN.(FFC)	
Pin1	NC
Pin2	GND
Pin3	NC
Pin4	Biometric_USBPN
Pin5	Biometric_USBPP
Pin6	3D3V S0

DQ15 AMD DIS SAMSUNG TI



## Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***F/P***

Size
A4

Document Number

Be

**QUEEN AMD Muxless/UMA<sup>00</sup>**

Date: Thursday, May 26, 2011

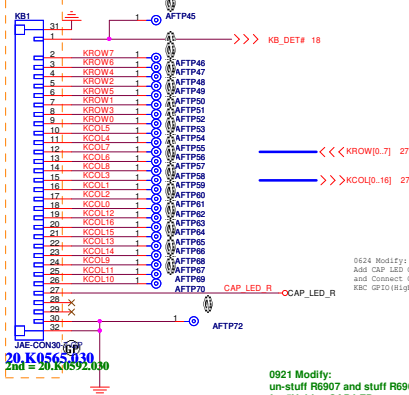
Sheet 64 of 104



1122 Modify:  
Add 2nd 20.K0592.030 on KB1 from ME  
updated connector list.

## Internal KeyBoard Connector

0630 Modify:  
Change KB1 part number to 20.K0565.030  
base on ME updated DBM and DDP.



<<< KROW[0..7] 27  
>>> KCOL[0..16] 27

0624 Modify:  
Add CAP\_LED Control circuit (Q6902, R6906, R6907)  
and Connect CAP\_LED\_R control to KB1 pin#27 from  
KBC GPIO (High active).

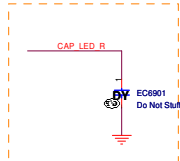
0921 Modify:  
un-stuff R6907 and stuff R6905, Q6902, R6906  
for 5V drive CAP\_LED.

0109 Modify: CAP\_LED Change To Low Active From KBC GPIO  
0109 Modify: R6905 Change To 1K

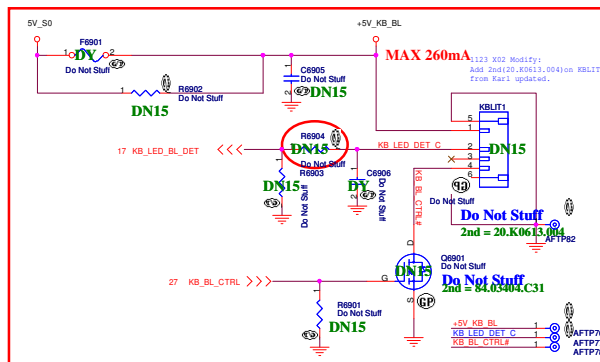
## CAP LED CONTROL



0719: EMI Request



## KB Backlight Connector

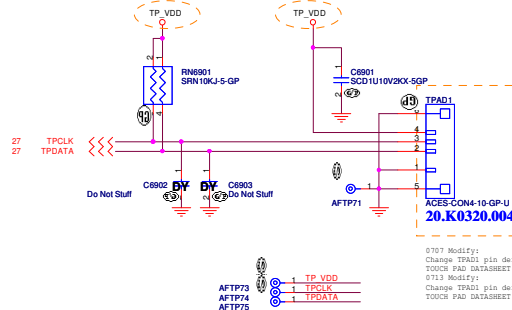


SSID = Touch.Pad

0624 Modify:  
Reserved TP LOCKED CONTROL combin  
with KEYBOARD Function Key.

0713 Modify:  
Change TPAD1 power source to 3D3V\_S0 from  
5V\_S0 based on DELL latest spec A02.

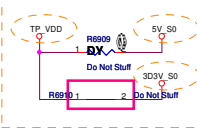
## TouchPad Connector



0630 Modify:  
Change TPAD1 part number to 20.K0320.006  
base on ME updated EMN&DXF.  
0712 Modify:  
Change TPAD1 part number to 20.K0320.004  
from 20.K0320.006.

0707 Modify:  
Change TPAD1 pin define to follow  
TOUCH PAD DATASHEET.  
0713 Modify:  
Change TPAD1 pin define to follow  
TOUCH PAD DATASHEET.

0715 Modify:  
Add R6908, R6909 for TPAD1 co-lay power option.  
0109 Modify:  
Change TP\_VDD To 3D3V\_S0, Follow Intel



MB CONN.	(FFC)
Pin 4	TP_VDD
Pin 3	TPCLK
Pin 2	TPDATA
Pin 1	GND

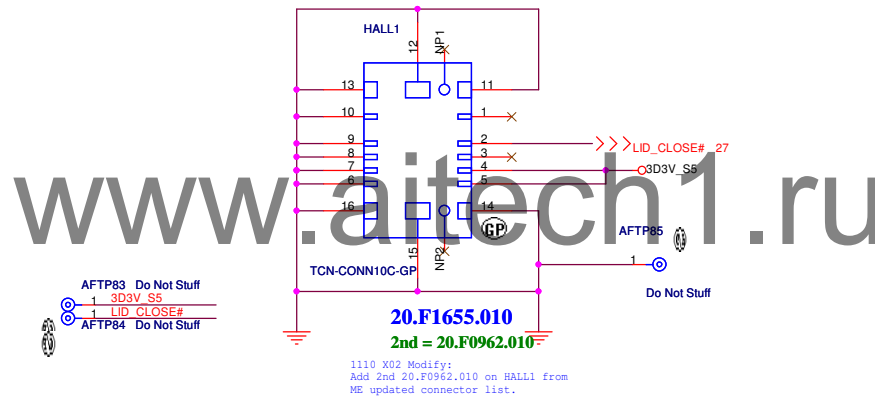
MB CONN. (FFC)	
Pin 1	+5V_KB_BL
Pin2	KB_LED_DET_C
Pin3	NC
Pin4	KB_BL_CTRL#

DQ15 AMD DIS SAMSUNG TI

SSID = Hall.Sensor

0906 Modify:  
HALL SENSOR move to small board at X01 stage,so  
Removed HALLSW1 related circuit and add HALL1  
connector.

1122 Modify:  
Add 2nd 20.F0962.010 on HALL1 from  
ME updated connector list.

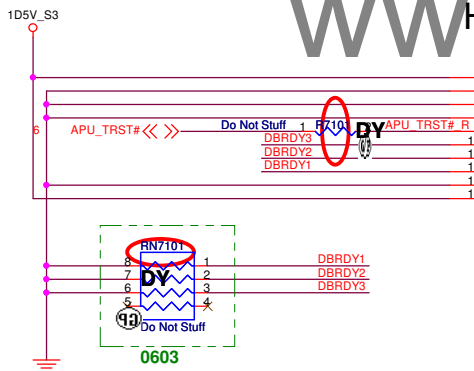


DQ15 AMD DIS SAMSUNG TI

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipet Hsien 221, Taiwan, R.O.C.	
Title			
Hall Effect Sensor			
Size A4	Document Number		Rev X00
Date: Thursday, May 26, 2011			
Sheet 70		of 104	



HDT+ Connectors  
HDT7101



```
CRB:placed 0-ohm
checklist:if both SCAN and HDT+ header are implement
placed 15-ohm
```

DQ15 AMD DIS SAMSUNG TI



Title

### Dubug connector

Size	A4
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Document Number

## QUEEN AMD Muxless/UMA

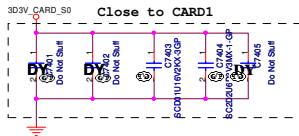
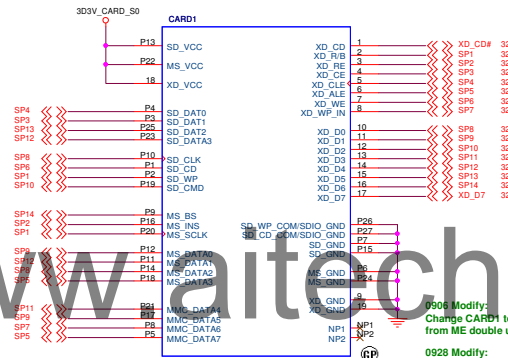
Rev	X00
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Date: Thursday, May 26, 2011

Sheet 71 of 100

104

SSID = SDIO

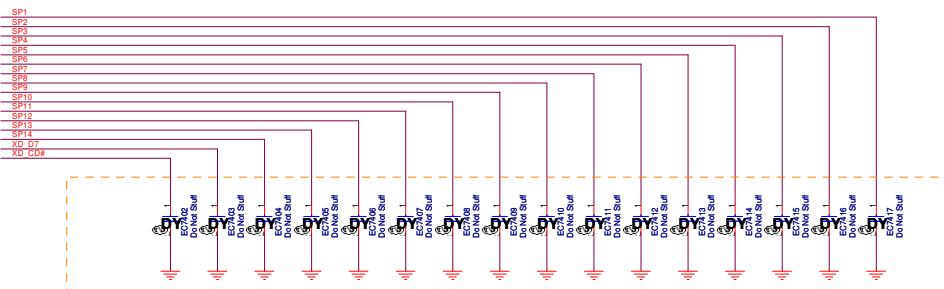
***SD/XD/MS/MMC+ Card Reader***

0906 Modify:  
Change CARD1 to 20.10129.001 from 62.10051.93  
from ME double updated latest DXF&EMN on X01

0928 Modify:  
Updated CARD1 footprint to R013-P12-HM-1  
from data base updated footprint.

1122 Modify:  
Add 2nd 20.10135.001 on CARD1 from  
ME updated latest connector list.

For EMI Reserved



0913: Schematic Score Card Suggest Cap Less Than 10P

20.10.29.001				
PH	TYPE	FUNCTION	RTS138 NET	
P1	SD	SD-CD	SP6	
P2	SD	SD-WP	SP1	
P3	SD	SD-DAT1	SP3	
P4	SD	SD-DAT0	SP4	
P5	MMC PLUS	MMC-DATA7	SP5	
P6	MemoryStick	MS-GRD	GND	
P7	SD	SD-GND	GND	
P8	MMC PLUS	MMC-DATA6	SP7	
P9	MemoryStick	MS-BS	SP14	
P10	SD	SD-CLK	SP8	
P11	MemoryStick	MS-DATA1	SP12	
P12	MemoryStick	MS-DATA0	SP9	
P13	SD	SD-VCC	3DV3 CARD SD	
P14	MemoryStick	MS-DATA2	SP8	
P15	SD	SD-GND	GND	
P16	MemoryStick	MS-INS	SP2	
P17	MMC PLUS	MMC-DATA5	SP9	
P18	MemoryStick	MS-DATA3	SP5	
P19	SD	SD-CMD	SP10	
P20	MemoryStick	MS-SCLK	SP0	
P21	MMC PLUS	MMC-DATA4	SP11	
P22	MemoryStick	MS-VCC	3DV3 CARD SD	
P23	SD	SD-DATA3	SP12	
P24	MemoryStick	MS-GND	GND	
P25	SD	SD-DAT2	SP13	
P26	SD	SD-WP COM	GND	
P27	SD	SD-CD COM	GND	
#1	XD	XD-CD	XD_CD#	
#2	XD	XD-R/B	SP1	
#3	XD	XD-RF	SP2	
#4	XD	XD-CE	SP3	
#5	XD	XD-CLE	SP4	
#6	XD	XD-ALE	SP5	
#7	XD	XD-WE	SP6	
#8	XD	XD-WP-IN	SP7	
#9	XD	XD-GND	GND	
#10	XD	XD-D0	SP8	
#11	XD	XD-D1	SP9	
#12	XD	XD-D2	SP10	
#13	XD	XD-D3	SP11	
#14	XD	XD-D4	SP12	
#15	XD	XD-D5	SP13	
#16	XD	XD-D6	SP14	
#17	XD	XD-D7	XD_D7	
#18	XD	XD-VCC	3DV3 CARD SD	
#19	XD	XD-GND	GND	

DQ15 AMD DIS SAMSUNG T



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1000

Size  
A3

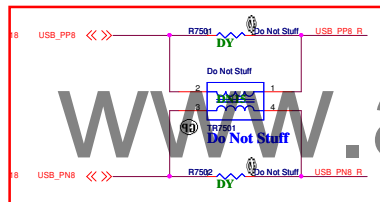
Document Number

**CARD Reader CONN**

Size A3	Document Number <b>QUEEN AMD Muxless/UMA</b>	Rev <b>X</b>
Date: Thursday, May 26, 2011	Sheet 74 of	104

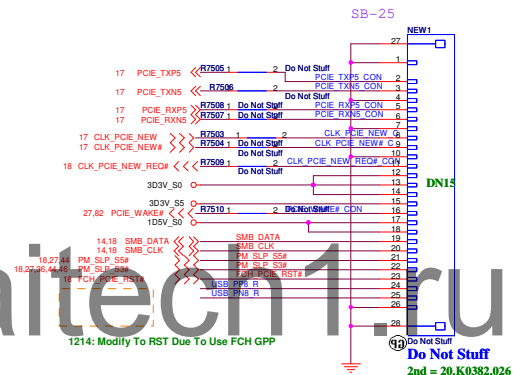
SSID = ExpressCard

1122 X02 Modify:  
Change TR7501 SW choke to 69.10103.041  
and un-stuff R7501, R7502 from BMC Neo Suggestion.  
Change R7501, R7502 to 9003 from 9402.  
1123 X02 Modify:  
SWAP TR7501 pin1&4 and pin2&3 each other  
base on Comite swap report.

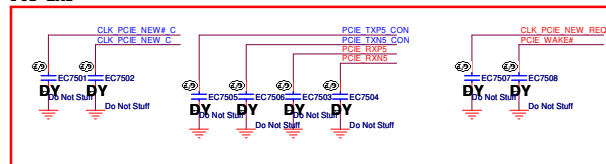


Do Not Stuff	AFTF107	1	3D3V_S5
Do Not Stuff	AFTF125	1	3D3V_S0
Do Not Stuff	AFTF110	1	1D5V_S0
Do Not Stuff	AFTF110	1	USB_PN8_R
Do Not Stuff	AFTF110	1	USB_PN8_L
Do Not Stuff	AFTF110	1	CLK_PCIE_NEW_REQ#_CON
Do Not Stuff	AFTF110	1	SMB_CLK
Do Not Stuff	AFTF110	1	SMB_DATA
Do Not Stuff	AFTF110	1	PM_SLP_S0#
Do Not Stuff	AFTF110	1	PM_SLP_S3#
Do Not Stuff	AFTF110	1	FCH_PCIE_RST#
Do Not Stuff	AFTF110	1	CLK_PCIE_NEW_C
Do Not Stuff	AFTF110	1	CLK_PCIE_NEW_C
Do Not Stuff	AFTF110	1	PCIE_TXNS_CON
Do Not Stuff	AFTF110	1	PCIE_RXNS_CON
Do Not Stuff	AFTF110	1	PCIE_RXNS_CON
Do Not Stuff	AFTF110	1	PCIE_WAKES_CON

1D5V\_S0\_CARD Max. 650mA, Average 500mA.  
3D3V\_S0\_CARD Max. 1300mA, Average 1000mA  
3D3V\_S5\_CARDAUX Max. 275mA



For EMI



DQ15 AMD DIS SAMSUNG TI

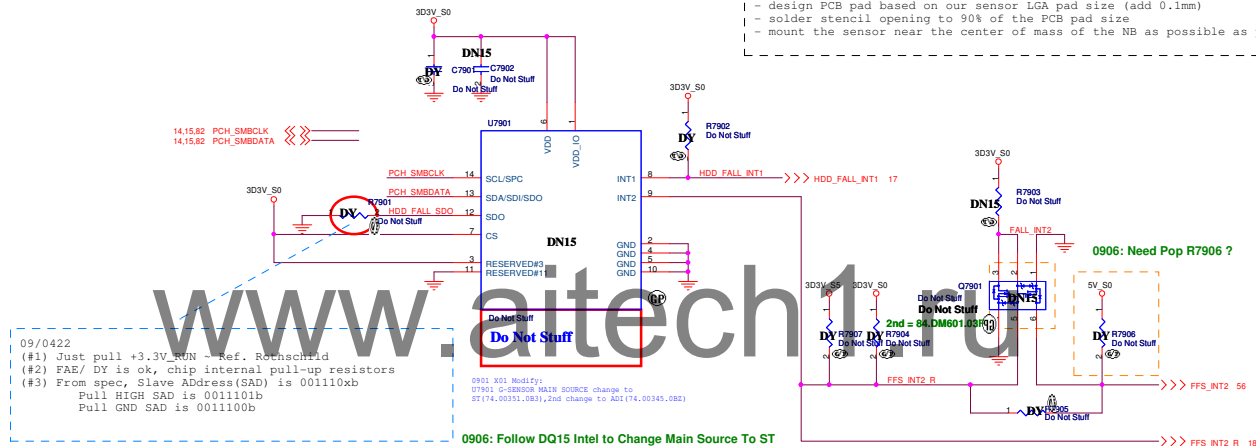
<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.			
<b>Express Card</b>			
File	Document Number		Rev
A3	QUEEN AMD Muxless/UMA		X00
Date: Thursday, May 26, 2011	Sheet	75	of 104

```
SSID = User.Interface
```

## Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note

- (1) Keep all signals are the same trace width. (included VDD, GND).  
(2) No VIA under IC bottom.

DQ15 AND DIS SAMSUNG TI



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TIME

### Free Fall Sensor

Size

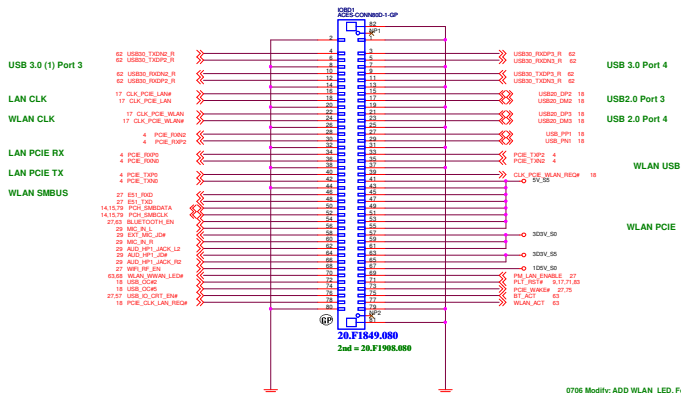
Document Number

Rev

**QUEEN AND Muxless/UMA<sup>®</sup>00**

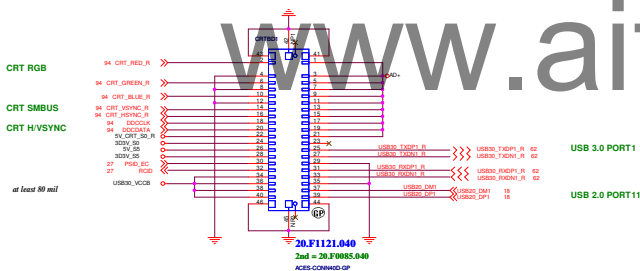
Date: Thursday, May 26, 201

Sheet 79 of 104



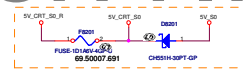
0706 Modify: ADD WLAN\_LED, Follow Intel, AMD Dont have WWAN

1123 Modify: Change Main Source To 20.F1849.080 & Add 2nd 20.F1908.080 on KBD1 from ME updated latest connector list & Modify Pin Define So 4 corner pin are GND.

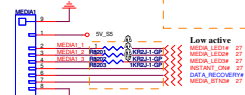
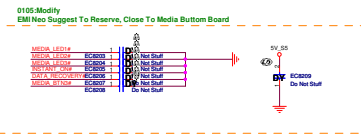


0914 Modify:  
Change B7B Connector To 20.F1121.040  
Follow ME Connector List  
1228 Modify:  
Remove USB 3.0 Signal and Re-arrange Pin-Define For Better Layout Routing  
1118 Modify:  
Modify Pin Define

0905 Modify:  
Change Part Number 20.K0422.010 To 20.K0320.008  
Base On ME Connector List  
0914 Modify:  
Change RS201~R8203 to 470 ohm from 33ohm  
for line tune MEDIA LED 5mA current.  
0925 Modify:  
Change RS201~R8203 to 430 ohm from 470 ohm  
for line tune MEDIA LED 5mA current.



0905 Modify:  
Change Part Number 20.K0422.010 To 20.K0320.008  
Base On ME Connector List  
0914 Modify:  
Change RS201~R8203 to 470 ohm from 33ohm  
for line tune MEDIA LED 5mA current.  
0925 Modify:  
Change RS201~R8203 to 430 ohm from 470 ohm  
for line tune MEDIA LED 5mA current.



ACIS-CONN-18-GP  
**20.K0320.008**  
1122 Modify:  
change Media resistor from 430 ohm to 1K on both DQDN15 (R8201, R8202, R8203) for Media button LED light spot issue

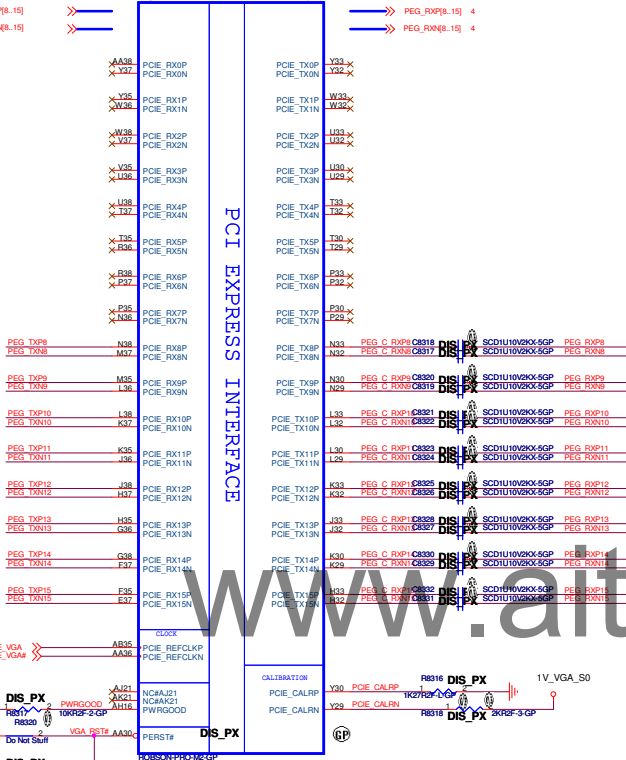
DQ15 AND DS15AUNG T1

4 PEG\_TXP[8..15]  
4 PEG\_TXN[8..15]

VGA1A

1 OF 8

PEG\_RXP[8..15] 4  
PEG\_RXN[8..15] 4



PCI EXPRESS INTERFACE

## CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0: Advertises the PCIe device as 2.5GT/s capable at power on. 1: Advertises the PCIe device as 5.0GT/s capable at power on.	0	1
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device won't be recognized as the system's VGA controller	0	0
ROMIDCFQ[2:0]	GPIO[13:11]	BIOS ROM EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0: Disable external BIOS ROM device 1: Enable external BIOS ROM device	X	0
VP_DEVICE_STRAP_EN	V2SYNC	VP Device Strap Enable indicates to the software driver that it sense whether or not a VP device is connected on the VP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]: 1:1 Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSXNC		X	1

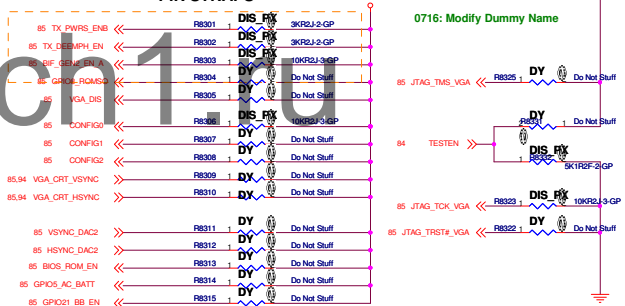
Full Tx output swing. Must be pulled to 3.3 V at reset using ~3K (5%) resistor.

DIS DY, CHECK

PIN STRAPS

3D3V\_VGA\_S0

3D3V\_VGA\_S0



## JTAG SIGNAL OPTION - for option2

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1" (PU)	"1" (PU)	"0" (PD)
JTAG_TRST#	"0" (PD)	"1" (PU)	NC
JTAG_TCK	CLK	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC

0113: Remove APU\_RST# Level Shift

1008: Add Level Shift For APU\_RST# To 3.3V

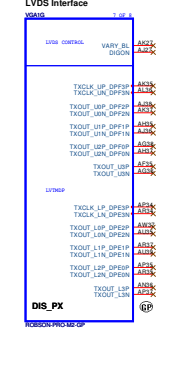
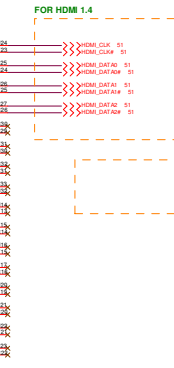
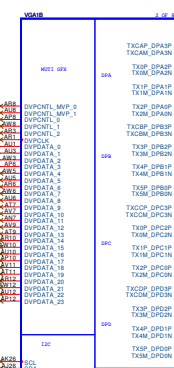
Q15 AND DIS SAMSLING TI

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GPU PCIe/STRAPPING(1/5)  
Size Document Number  
Custom QUEEN AMD Muxless/UMA  
Date: Thursday, May 26, 2011  
Sheet 85 of 104

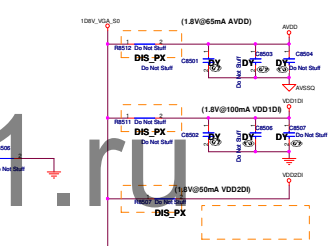
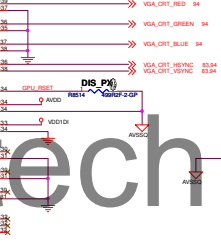


VPDATA[3:0]	Description	FN
0001	DDR3 Hynix-H5TQ1G63BFR-11C (900MHz) 128M*16	72.52G63.A0U
0011	DDR3 Hynix-H5TQ1G63BFR-11C (900MHz) 64M*16	72.51G63.A0U
0010	DDR3 SAMSUNG-K4W2G16460-BC11 (900MHz) 128M*16	72.42164.Q0U
0000	DDR3 SAMSUNG-K4W1G16460-BC11 (900MHz) 64M*16	72.41646.Q0U



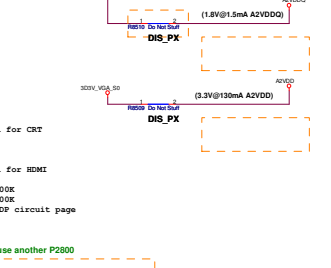
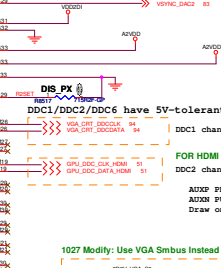
0708: Need To Pick GPIO  
0708: Add Thermal Shutdown Circuit  
0107: SW Will Not Use This Function, DY For Reserve Only

I2C Bus for LVDS



0112: Dummy Cap

### 0112: Remove Cap



**Clock Input Configuration -GDDR3/DDR3**

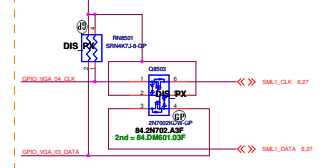
- a) 27MHz crystal connected to XTALIN or XTALOUT or
- b) 27MHz (1.8V) oscillator connected to XTALIN or
- c) 27MHz (3.3V) oscillator connected to XO\_IN (Park, Madison, and Broadway only)

tolerant

DDC2 channel for HDMI

AUXP PD 100K  
AUXN PU 100K  
Draw on EDP circuit pag

1027 Modify: Use VGA Smbus Instead of use another P2801







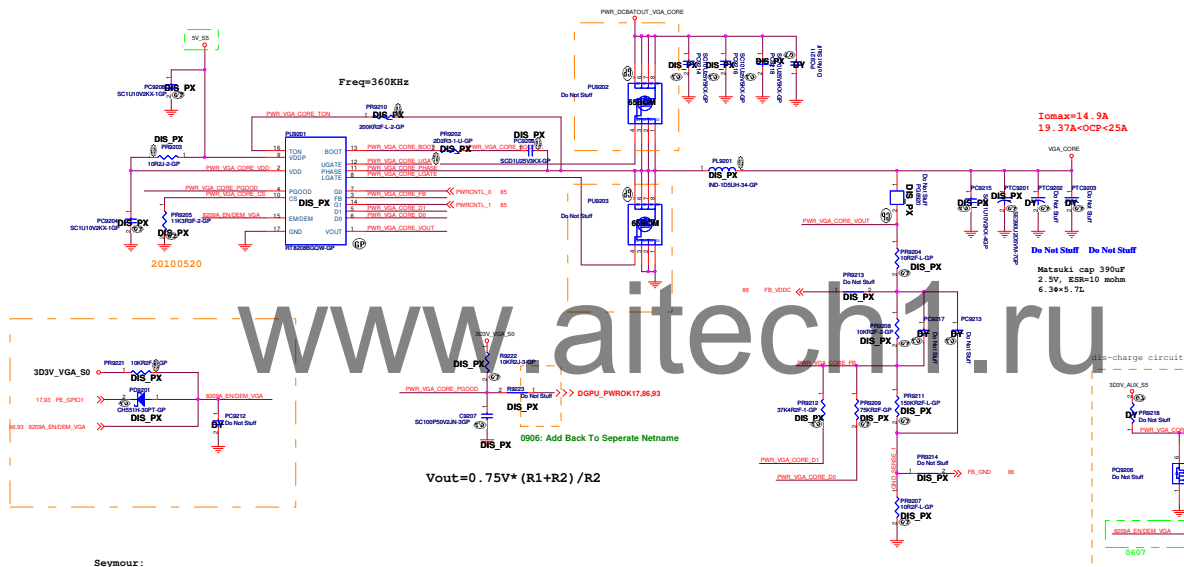












Seymour :

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.1V
L	H	1.0V
H	L	0.9V
H	H	X

Whistler :

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.0V
L	H	X
H	L	0.9V
H	H	X

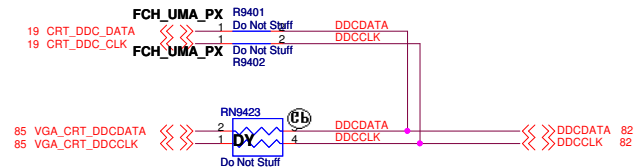
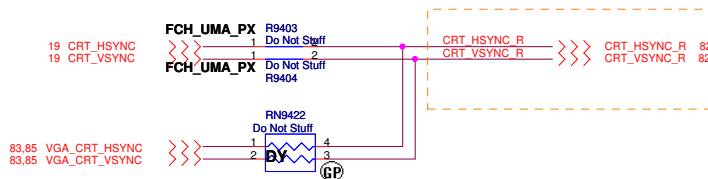
	999208	999211	999209	999212
Seymour	10GR2F	15GR	75GR	27W4R
Whistler	10GR2F	75GR	75GR	15GR

I/F cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: 1.5uH PFCM104T-1R5MH Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J  
O/P cap: 560U 2.5V MP2VL560MCSR7 16mOhm 3.5Arms 77.55671.00L  
O/P cap: 220U 2V EFCFC0D221R 15mOhm 2.7Arms Panasonic/79.22719.20L  
H/S: RJK03B9DPA / 10.9mohm/15.1mOhm@4.5Vgs 84.003B9.B37  
L/S: RJK03D4DPA / 4.6mohm/5.6mOhm@4.5Vgs 84.00034.A37

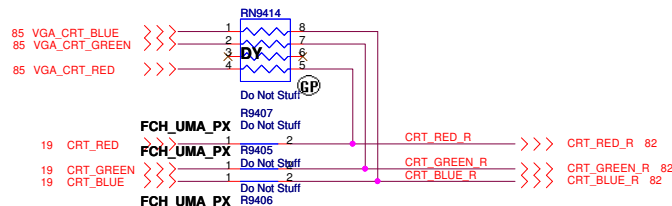




SSID = VIDEO

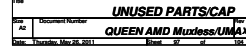


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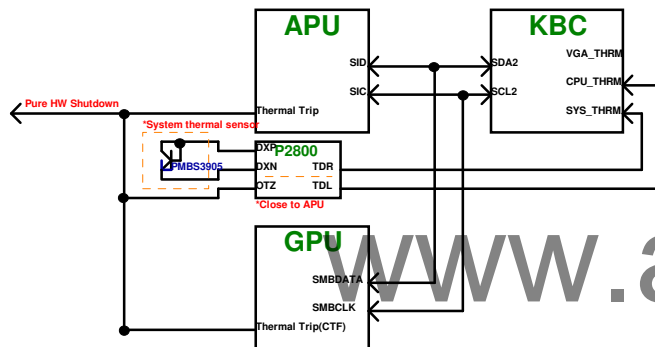


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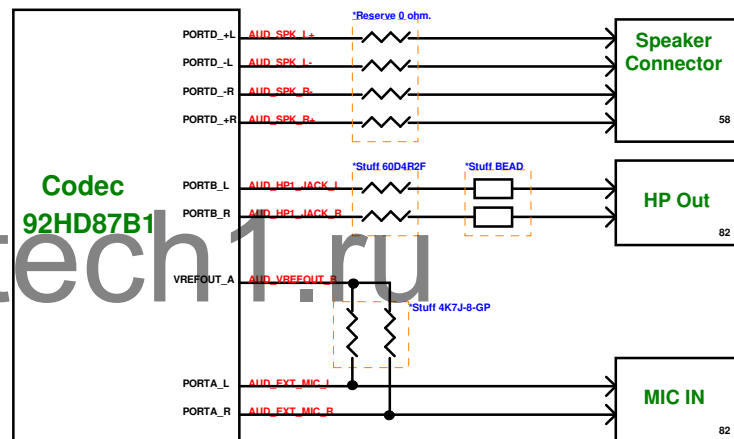
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>LVDS VGA Switch</b>			
Size	Document Number		Rev
	<b>QUEEN AMD Muxless/UMA</b>		<b>X00</b>
Date: Thursday, May 26, 2011		Sheet 94	of 104



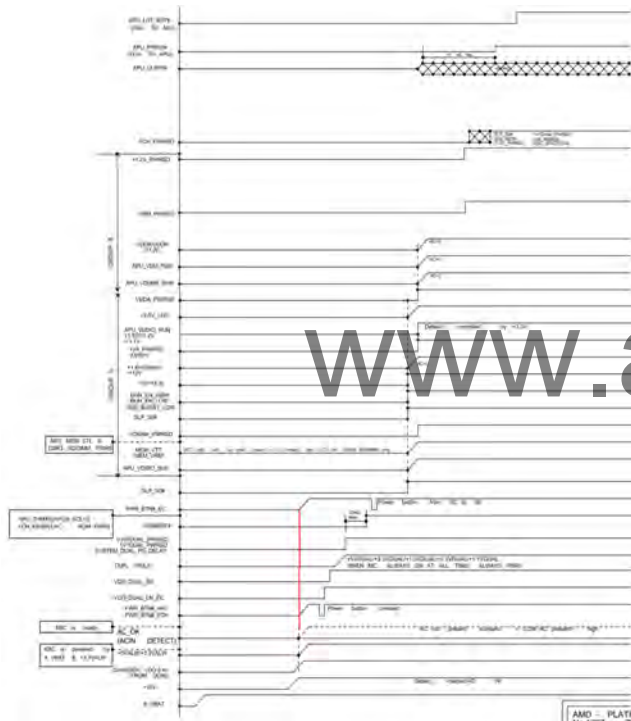
## Thermal Block Diagram



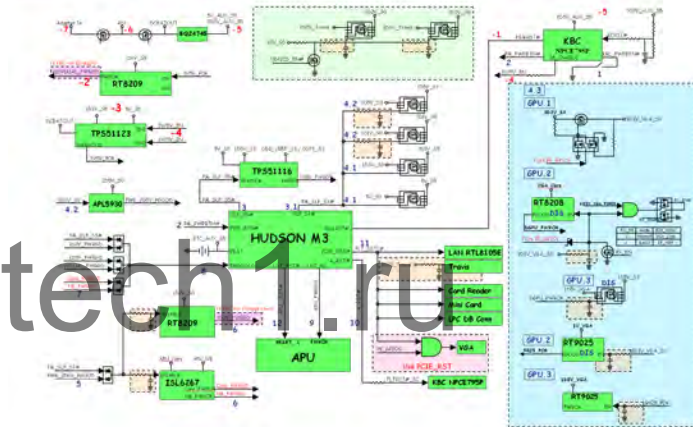
## Audio Block Diagram



# POWER SEQUENCE

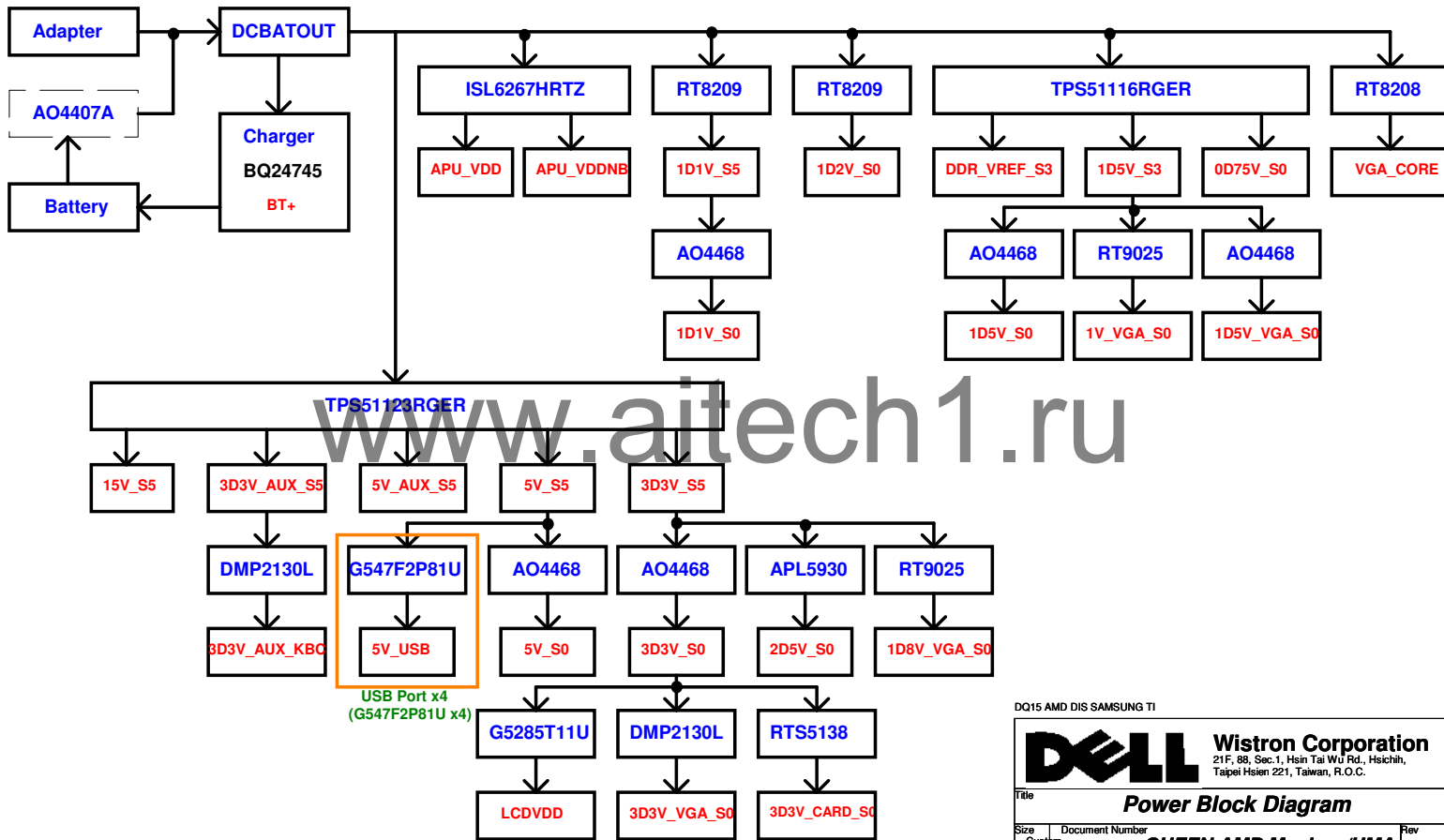


## SABINE ROSA Sequence (Adapter In)



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0015 AND 0016 00000000



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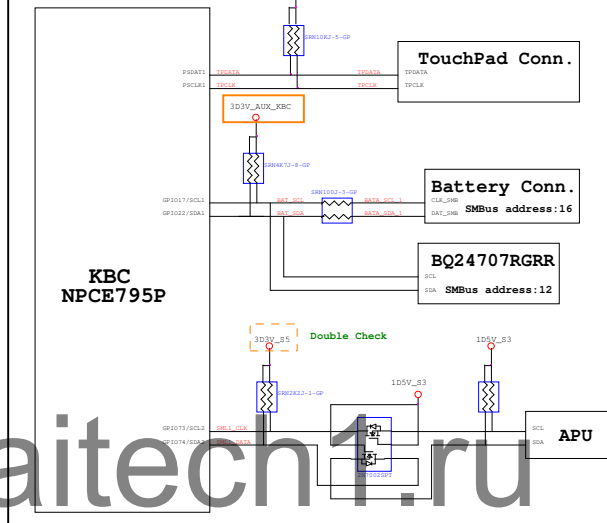
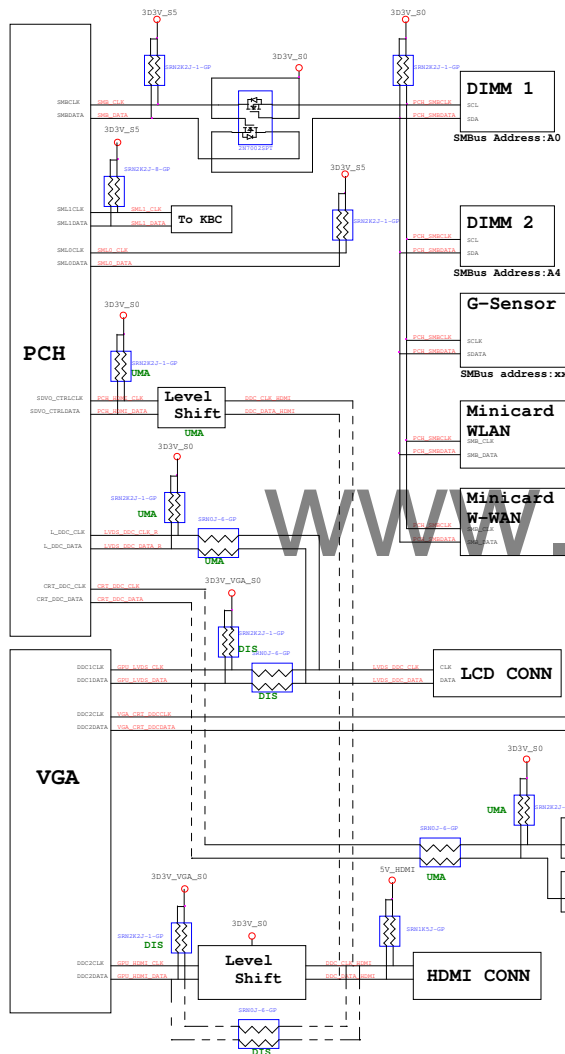
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Title **Power Block Diagram**

Size Custom Document Number **QUEEN AMD Muxless/UMA** Rev **X00**

Date: Thursday, May 26, 2011 Sheet 100 of 104

### KBC SMBus Block Diagram



## Change notes - Page 4

VERSION	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X02	01/08	3	18, 19	Add C1825,C1922.	Reduce V_REF ripple by EA team result.	EE
		4	37	Reserve C3721,C3722.	Prevent signal cross talk.	EE
		5	ALL	Change capacitors value and add C3723.	Ensure signal quality.	EE
	01/11	1	68	Change KB1 P/N.	According ME request.	ME
		2	66	Change R6601,R6602,R6604,R6606 to 1KR, R6603 to 470R.	Decrease LED brightness.	EE
	01/12	1	37	Add C3724, R3757.	To set accurate current detection in EC.	EE
		2	10	Add R1041 0R.	Add 0R for level shift off.	EE
	01/13	1	21, 37	Add C3725, C2105.	Reserve for singal quality.	EE
	01/14	1	Power	Modify power team componets.	Request by Power Team.	Power
		2	7	Change RN712 to 22R.	Fine tuned damping resistor value.	EE
A00	02/08	1	66	Reserve R6609, R6610 1KR.	Add for future LED brightness balance.	EE
		2	68	Add keyboard back light circuit, remove R5403.	Add for keyboard with back light module.	EE
		3	69	Change HALLSW1 footprint for co-layout.	Change for co-layout different kind of HALLSW1.	EE
		4	77	Add AFTP7701, AFTP7702, AFTP7703.	Add AFTP test point for factory test.	EE
	02/10	1	Power	Update Obsolete parts.	Update obsolete parts due to policy.	Power
		2	79	Change HBT1 part number.	Change HBT1 part number to match ME EMN file.	ME
		3	47	Add PTC4710.	Add to solve board acoustic issue.	EE
	02/22	1	54	Remove co-layout pad.	As factory request.	EE
		2	42	Add C4217, C4401, C4402.	Ensure signal quality.	EE
		3	48	Delete Power Gap.	Request by Power Team.	Power
	02/23	1	ALL	Change to short pad.	Change most of 0-ohm resistors to short pad.	EE
	02/24	1	7, 68, 79	Reserve C724, C725, C6806, C6807, EC7928-EC7932.	As EMC team request.	EMC
	02/25	1	13	Add TP1309.	As factory request to add.	Factory
		2	7, 68	Rename EMC capacitor to EC704, EC705, EC6801, EC6802.	Meet schematic standardization.	EE
		3	49, 89	Change PR4913 to 3.9R, PR8905 to 6.98KR.	PR4913 for snubber, PR8905 for OCP.	Power
		4	21	Change R2133 to 0R.	Set GPIO input level from 0.5V to 0V.	EE
		5	79	Remove EC7928.	Layout space limitation.	EE
	02/26	1	39, 42	Empty R3906 and Change R4202 from 0R to 1KR.	It is for solving T8 shutdown issue.	EE
	03/03	1	60	Change SPK1 part number.	Request by ME.	ME
	03/05	1	20, 24, 37	Empty R2029, R2404, R3751.	Saving unused components.	EE

0303-1

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Title	Change notes	
Size / 33	Document Number QUEEN AND MURDER/UMA	Rev X00
Date: Thursday, May 26, 2011		
Sheet 103 of 104		